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On the Cover....

SEM micrographs show dice which were apparently damaged during the die bonding operation. Both devices failed PIND testing and silicon particles were retrieved from each. Loose conductive particles present a risk of performance degradation or catastrophic failure.

(Picture and description courtesy of Chris Greenwell of the GSFC Parts Analysis Laboratory)

WWW URL Address:

http://arioch.gsfc.nasa.gov/eee_links/eeeintro.html

LETTER FROM THE EDITOR

by Melanie Ott
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Due to the many distractions of this year which include several government furloughs and a blizzard, we are publishing the first quarter issue of *EEE Links* later than anticipated. The next issue will be released during the June/July summer months.

We will no longer be emailing the newsletter due the increasing size. This issue in particular has many diagrams, graphs and tables. In providing this type of information we generate large files that may aggravate email systems and severely upset system administrators. If you need to be on hardcopy distribution because you don't have access to the World Wide Web, contact me. Otherwise, for now, hardcopy distribution will continue and the newsletter will be available on the WWW at the address:
http://arioch.gsfc.nasa.gov/eee_links/eeeintro.html
If you are having accessing problems you can always contact Doug Smith at 301-286-0695.

In case you were wondering, Michelle Davis, Chris Reiher and Doug Smith have gone on to other opportunities and are no longer part of the *EEE Links* staff. Therefore, for all future subscription information and article submissions please contact me at the above phone number or email address.

My apologies for publishing the incorrect fax number in the last issue of *EEE Links* and to anyone who had trouble getting their communications through due to Michelle's departure. The correct fax number is 301-731-8603. Please be very sure to indicate that your fax is in reference to *EEE Links*.

I would like to extend a very special "Thank You!" to the knowledgeable authors who write for *EEE Links*, especially some of our regulars: Dr. Reza Ghaffarian (JPL), Richard Katz (GSFC), Richard Karpen (JPL Parts Analyses), Nick Virmani (GSFC/Unisys), Don Nichols (JPL), Dr. James Chern (GSFC), Dr. Kusum Sahu (GSFC/Unisys), Doug Smith (GSFC/Unisys) and Chris Greenwell (GSFC/Unisys) for contributing cover pictures. It takes a large team to create *EEE Links*. Your efforts are much appreciated!

JPL'S SEE TEST AT TEXAS A & M

November, 1995

by Donald K. Nichols
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A single event effects (SEE) test was held at the new Texas A&M Cyclotron SEE facility on November 16-18, 1995. The list below describes the devices and parameter used during testing conducted by JPL at this facility.

1) A set of linear devices: NSC LM139, NSC LM111 & PMI LM139 comparators; and LTN RH1056, LM108A & RH108A op amps were tested for SEE-induced transients. TAM provided 1961 MeV Xe with LET=44 MeV/ (mg/cm^2)and 600 MeV Ar with LET = 7.3 MeV/(mg/cm^2). Significant transients were observed--voltages often rail-to-rail (+/- 15V), pulse durations of approximately 1 to 20 microseconds and LET thresholds always much less than 7.3 MeV/(mg/cm^2).

2) A latchup test of Intel 28F016SA & 28F016SV (smart voltage) was conducted. The 16 Mbit flash memories showed a common latchup threshold of 44 MeV/(mg/cm^2). The test was for a program voltage of Vpp=12V only.

3) The Mosaic MDM14000GMB-80 package of a Mitsubishi die M5M44100 showed no latchup up to an effective LET=87 MeV/(mg/cm^2), for temperatures of up to 53 degrees C.

4) Harris 2N6764, Phillips ECG2392 and Siliconix VN88AF n-channel power MOSFETs were tested for SEB and SEGR. All exhibited failure in the mid to upper range of operating voltage.

5) A latchup test of the Burr Brown DDC101 20-bit analog-to-digital converter showed a latchup LET threshold of 9 MeV/(mg/cm^2).

"DOC"

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In January of this year, the space passive parts world lost one of its leading figures when Doctor A.M. (Doc) Holladay passed away. Doc worked at the Marshall Space Flight Center from 1964 to 1984 as an electronics parts specialist. It was there that he made his best known contribution to the reliability of space flight electronics.

From 1971 to 1975 he managed the development effort to find an interchangeable replacement for the failure prone, silver-cased, wet slug tantalum capacitor. The result of this effort was the highly successful CLR79 style capacitor that is still in widespread use by NASA, the Air Force and civilian space enterprises. Doc made major contributions to the knowledge of tantalum capacitor performance and reliability factors and wrote several valuable papers on these subjects. After his retirement from NASA in 1984 Doc remained active in the parts world as a consultant and continued to write and present papers. Until last year he was a familiar figure at the annual Capacitor and Resistor Technology Symposia (CARTS). He will be greatly missed, especially by people in the parts world.

VIBRATION EVALUATION OF A CIRCULAR CONNECTOR WITH OPTICAL CONTACTS

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The use of a multi-termini optical connector in a fiber optic application has been adopted on two GSFC programs. This connector system introduces the use of individually removable, specially polished, physically contacting, optical contacts. An evaluation was performed to address this connector's performance in a vibration environment when used for fiber optics. The connector's optical performance was found to be acceptable although deficiencies were found regarding generation of contamination.

The connector pair evaluated was Amphenol- Bendix's TVS style miniature circular type (akin to the military's MIL-C-38999 family of connectors) assembled with four MIL-T-29504 optical contact pairs. The contacts terminated Brand-Rex S-311-P-339/1 fiber cable; the type used by GSFC in space flight hardware. The connector assembly was thermally soaked and cycled between -55°C and 85°C prior to vibration testing. The standard MIL-STD-1344, Method 2005, Condition V (18.7 Grms, 6 minutes in each of three mutually perpendicular directions) was used for vibration. A second vibration test was performed using a bracket which exposed the connector to over 37 Grms using the same military test procedure. Continuous optical sampling of the four channels, during testing, was used to identify reduction or loss of signal.

The results showed that the connector performed within the manufacturer's specifications to at least 37 Grms random vibration, with thermal cycling preconditioning. Contamination was found to be generated by the connector itself, indicating the need for attention to cleanliness and the development of adequate cleaning procedures. Alignment sleeve retention force played a role in the occurrence of metal filing contamination between one of the optical contact pairs, indicating that alignment sleeve retention force should be more closely controlled. Finally, the optical contacts with less than ideal polish qualities tended to degrade over the duration of the evaluation which indicates that cleave and polish damage can lead to increased polish surface defects over the life of the optical connector.

While the connector was found suitable for use in environments that experience mild thermal cycling, further study of the relationship between the surface polish defects, temperature and fiber tension can show their suitability for use in more thermally stressful environments.

GSFC EEE PARTS CATALOG

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Goddard Space Flight Center, Code 230 has published a catalog of EEE parts that are available through the logistics contractor, Code 239. The catalog contains about 3500 different EEE parts (mostly resistors, capacitors, connectors, and microcircuits) that are in stock, or that can be obtained through Code 239.

Please note that there are no overhead charges added to the prices of items acquired through through the Code 230 stores stock system. The prices paid by the logistics contractor are passed on directly to the user, with no additional mark-up.

The catalog divides the parts into two major subsets, engineering-level and flight-level. For flight-certified items, all technical, certification, and lot-date information is available from Code 239.

The catalog was published in 1995, and additional items have been cataloged in the meantime. Therefore, other items, especially flight fasteners, not shown in the catalog may also be available.

The catalog is available from the Code 300 technical library, or from Ms. Patricia Gilbertson, Code 239,. 301-286-9556.

If you have additional questions about the Code 230 EEE parts and fastener programs, please call any of the following:

- Patricia Gilbertson, Code 239, 301-286-9556.
- Bob Clark, Code 235, 301-286-7740, or;
- Glenn Harris, Code 235, 301-286-3385.

TECHNOLOGIES SEMINAR PROGRAM AT GODDARD SPACE FLIGHT CENTER

by Robert Savage,
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The Assurance Technologies Division of Goddard Space Flight Center has announced the start of a Technologies Seminar Program. The seminar will cover a variety of topics including parts, packaging, testing and other new related technologies for space flight hardware. The first seminar will cover the capabilities of the Assurance Technologies Laboratory located in building 6 at GSFC. Please join us in room S-19 of building 6 on March 25, 1996 from 9:00am to 11:00am. If you will be in GSFC vacinity on March 25 please contact Melanie Ott, 301-731-8644 for directions and arrangements to attend.

ROBUST DESIGN TECHNIQUES AS APPLIED TO ELECTRONIC PACKAGING AND FABRICATION PROCESSES

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The evaluation and qualification of electronic packaging for NASA space vehicles is an involved and lengthy process. There are so many variables which affect the overall reliability of interconnections such as solder joints, that testing for the effects of these parameters could be a never ending assignment. The principals of robust design as formulated by Dr. Genichi Taguchi offer the opportunity to reduce the process of test and evaluation for electronic packaging and fabrication advancements. Robust Design, or as often known as Taguchi Methods, is a unique engineering optimization process that unifies the improvement of quality, reduction of cost, and reduction of product development time.

Recently at JPL the Robust Design (also known as Designed Experiments) techniques were successfully employed in several research, development, test and evaluation processes including new spacecraft battery technology research and development , spacecraft battery operation management optimization, direct methanol fuel cell research and development, and other currently on-going applications.

These same techniques are now being employed in the area of electronic packaging and manufacturing. The NASA desire to launch many small, less expensive exploratory spacecraft is driving the electronic designers to more compact electronic assemblies made possible by advances in the packaging arena. Area Array Packages including Ball Grid and Column Grid Arrays hold great promise into the miniaturization of spacecraft electronics. Direct chip attachment techniques such as chip and wire and flip chip technologies will possibly provide the next quantum leap into compacting the electronic assemblies by eliminating the chip package and attendant interconnecting systems. We, in the packaging and fabrication fields, must find the optimum methods and materials to provide high reliability to the electronic assemblies which use these advances. Each of these new technologies bring with it a set of parameters to be optimized to insure the reliability level required of the mission. In the case of chip and wire technology, as an example, the substrate materials, plating of bonding surfaces and surface finishes, wire bond schedules and technique (ultrasonic and thermosonic), composition and thickness of wire, and encapsulation material and methods are all parameters to be evaluated over the various possible levels. Robust Design provides the methodology to reduce the required number of laboratory tests to a minimum.

The development of the Robust Design orthogonal array to be applied to a particular packaging technique begins with the determination of all of the parameters which could affect the result. In this case the result is defined as the overall reliability and lifespan of the assembly when exposed to temperature cycling commonly experienced by our spacecraft. Continuing with our example of the chip and wire style of directly attaching chips to printed wiring boards, we could have identified the parameters and their respective levels as shown in table I. Since the effort to evaluate Direct Chip Attach Technology at JPL is in the very earliest stages of planning, it is not presumed that Table I has captured all of the pertinent parameters or even the most important. It is presented as an example only.

TABLE 1
Example-Chip and Wire Direct Chip Attach Parameters and Levels

Parameter	Level
A. Printed Wiring Board Material	1. Polyimide
	2. Aramide constrained polyimide
B.Plating of Wire Bond Pads- PWB	1. Gold over copper
	2. Gold over nickel over copper
C.Plating of Wire Bond Pads-Chip	1. Gold
	2. Aluminum
D.Wire Bonding Methods	1. Ultrasonic
	2. Thermosonic
E.Wire Composition	1. Gold
	2. Aluminum
F.Encapsulation Material	1. Organic
	2. Inorganic compound
G.Substrate mounting Pads for chip	1. Gold over copper
	2. Gold over nickel over copper

In this simple example of direct chip attachment, there are 7 parameters of interest each with 2 levels. Testing all possible combinations of these parameters and levels would require 2 to the 7th power or 128 experiments. The 128 experiments would, in this case, represent the full factorial in which the optimal performance combination would be tested and, thereby, identified. Dr. Taguchi has developed and published the 20 most commonly used fractional factorial of these test parameters, referred to as the orthogonal arrays. Among these, the L8 is the orthogonal array which will lead to the same optimized combination resolution through only 8 experiments. Table II shows the 8 experiments defined by this array.

TABLE II
Definition of Experiments-Orthogonal Array for Direct Chip Attachment Example

Experiment	Parameter						
	A	B	C	D	E	F	G
1	A1	B1	C1	D1	E1	F1	G1
2	A1	B1	C1	D2	E2	F2	G2
3	A1	B2	C2	D1	E1	F2	G2
4	A1	B2	C2	D2	E2	F1	G1
5	A2	B1	C2	D1	E2	F1	G2
6	A2	B1	C2	D2	E1	F2	G1
7	A2	B2	C1	D1	E2	F2	G1
8	A2	B2	C1	D2	E1	F1	G2

As a matter of explanation, experiment 1 in this array would be run on a sample with all 7 parameters set at level 1. The printed wiring board would be polyimide, the bonding pads on the PWB would be gold plated, the chip would have gold bonding pads, ultrasonic wire bonding would be used, etc.

After the 8 test samples are constructed in accordance with the parameter levels defined in the orthogonal array, the actual tests are performed to determine reliability levels. In the case of electronic packaging for spacecraft, the traditional testing is thermal cycling from -55 degrees C. to +100 degrees C. until electrical failure of the interconnections occurs. In the language of Robust Design, the thermal extremes and cycles experienced by the electronics in a real mission is the "noise" (i.e. the uncontrollable element) which the hardware is to be designed with enough robustness to withstand.

The data gathered through the test phase is entered into a software package which, through the magic of statistics, separates the effects that each of the parameters has on the overall reliability of the product. The designer then selects the level of each parameter which has been shown to contribute most positive effects to the overall reliability. The optimum combination of these parameter levels is very likely to be one which was not represented in the orthogonal array since only 8 of the possible 128 combinations were included. The final phase of the process, therefore, is the confirmation experiment in

which the identified optimized combination is built and subjected to the thermal cycling tests. The reliability of this test sample should be greater than that of all of the sub-optimal samples included in the array. In the experiments actually performed at JPL to date, this has been the case.

At the Jet Propulsion Laboratory, Taguchi defined methods of Robust Design that have been employed to help design and optimize a number of different products including batteries and fuel cells have performed quite successfuly. These methods are now also used in the areas of electronic packaging and fabrication. Currently programs, largely funded through Code Q RTOPs , in Surface Mount Technology and Area Array Packaging are benefiting from these techniques. Other packaging endeavors such as Direct Chip Attachment which are just in the planning stages will use Robust Design to speed up the qualification for use in NASA space vehicles.

ISWG INFORMATION EXCHANGE

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The ISWG (Interconnection Standardization Working Group) Information Exchange is a column provided in every issue of EEE Links to keep the NASA community informed of the recent concerns and developments in the areas of interconnection, wire, cable, and fiber optics.

- The conference proceedings from the Third NASA Workshop on Wiring for Space Applications have been sent out. Workshop Chair, Ahmad Hammoud can be reached at 216-433-8511. To receive a copy of the proceedings you can contact the NASA Center for Aerospace Information at 301-621-0390.
- The EIA Special Task Group on Space Requirements met in Tucson, Arizona in February. Due to the many yellow ballot comments submitted during the recent circulation of the connector baseline, *Guide of Space Requirements for Electrical Connectors PN-3514*, the committee decided that once all comments have been incorporated, the document will once again be reviewed before proceeding to the standards proposal stage. For more information please contact me.
- The 100/140 micron fiber optic cable OC-1008 previously fabricated by Brand Rex with Corning fiber has been discontinued. This fiber was being used by NASA Goddard projects and was listed on their preferred parts list. Code 311 at Goddard is looking into alternatives to replace this cable for space flight applications. Spectran is providing a cable that is similar to the OC-1008 with differing buffer dimensions and materials to the NASA Training Center for training purposes only. This fiber has not yet been qualified for space flight. Spectran encourages use of their Flight-Guide cable which has a hermetic/ polyimide coating that must be removed with hot sulfuric acid. Without removing the coating, a non standard connector will have to be used. The MIL-STD-1773, SEDS II Module uses this type of fiber and is used in a pig-tailed fashion.

SOLDERABILITY TEST AND CORRELATION TO SMT SOLDER JOINT QUALITY

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Ultra-low volume Surface Mount Technology (SMT) assemblies for space applications do not permit proof of process as do commercial or military production quantities. This fact mandates that Quality Assurance (QA) involvement be proactive and be included throughout the process of validation, proof of process build, and problem detection by inspection. The QA engineer should be responsible for ensuring that manufacturing controls are in place and that critical inspection steps are considered and understood.

There are four concurrent SMT RTOPs (Research, Technology Objectives and Plans) aimed at developing a coherent design and qualification methodology for SMT utilization in NASA hardware, including those at the Jet Propulsion Laboratory. Each RTOP addresses a different aspect of SMT. These include design, manufacturing, test, reliability modeling, and QA methodologies. The objectives of the Quality Assurance Methodology RTOP are to identify the critical parameters of SMT manufacturing and determine the methods and tools required to integrate QA procedures into the design and manufacturing processes so that the critical parameters may be bounded and controlled

In an SMT survey performed in NASA centers in 1993, one of the key cause of SMT solder joint rejects was attributed to solderability issues. To address this issue realistically, solderability of lead remnants after lead forming were compared to the solder joint quality of the same package leads after assembly. Fine pitch 0.20 inches gull wings were used for evaluation. Solderability

tests were performed on 25,000 solder joints in strips of 64 leads (one side of 256 leads) and 41 (one side of 164 leads) using a quantitative Multicore Universal Solderability Tester (MUST). This measures wetting force against time while a specimen is dipped into molten solder. The dipping can be either done manually or with the aid of external computer control.

Twenty strips were also subjected to the dip-and-look qualitative test method. The dip-and-look method has been used since 1950 and is the basis of MIL-STD-202, Method 208 and EIR-RS-178. It is still widely used today. The military standard requires 95% coverage of a lead after dipping in a standard hot solder bath.

Table 1 lists dip-and-look, MUST print out test data and solder joint inspection results. Values for dip-and-look are approximate area percentages of non-coverage solder areas. F, r, and S parameters are those read from MUST print-outs. These parameters are automatically calculated based on the wetting section of the curve, i.e., time to begin wetting to time to maximum wetting force.

The plot portion approximates to an exponential, that is the force f at any time t is considered to be a function of the maximum force Fmax and the time constant S.

$$\mathbf{f = F_{max}\ (1 - exp(-t/S))}$$

The "wetting speed" changes with time and is a function of the time constant S. The force f changes from the maximum negative wetting force to the maximum positive force. S is measured in seconds, when t = S then $f = 0.632\ F_{max}$. F_{max} and S can be calculated from the force/time curve. The MUST wetting balance takes force readings every 0.1 seconds, and computes the best fit of data to a straight line of log-log of this equation. The value F_{max} and S are calculated from the regression line together with the coefficient of correlation r, which express how closely the observations fit a straight line.

The output values of r, S, and F give some indication of solderability. The r (dimensionless) indicates uniformity of wetting and should exceed 0.8 when wetting is uniform. S, in seconds gives some indication of the speed of wetting. A value of less than 1 second shows rapid wetting which is considered to be good. The total wetting force, F, depends on the perimeter of the specimen and, when divided by the perimeter value in mm, gives the wetting strength.

Based on the dip-and-look test results, all of the 164 and most of the 256 gull wing leads failed solderability testing (non-coverage area more than 5%). Results of solder joint assembly inspection contradict the dip-and-look test results for the 164 gull wing leads whereas they agree with the results of the 256 leads. It should be noted that the 164 leads had a tin coating layer whereas the 256 leads had a gold coating layer. It is possible that the test results were influenced by the surface coating conditions. This needs to be further explored.

The research described in this publication is being carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. For more information on this, contact the author.

TABLE 1 Lead Solderability Test Results And Solder Joint Inspection

Serial Number	Time Constant (sec)	Correlation Coefficient	Wetting Balance Force (grams)	"Dip & Look"non-coverage	Dip & Look Pass/ Fail	Solder joint Visual Inspection
164 GW	**S**	**r**	**F**	**(%)**		
6	.407	.951	.734	25	Fail	OK
9	.258	.966	1.060	10	Fail	OK
32	.269	.970	.579	10	Fail	dewet,nonwet
36	.569	.876	.367	20	Fail	OK
62	.334	.964	.541	25	Fail	No inspection
68	.543	.855	.509	35	Fail	OK
69	.797	.741	.906	30	Fail	dewet
79	.881	.933	.538	15	Fail	dewet
256 GW						
1024	.357	.971	1.320	5	Pass	OK
1034	.346	.962	1.126	1	Pass	OK
1035	.413	.916	1.426	20	Fail	bridge
1037	.410	.866	1.518	30	Fail	open
1044	1.205	.426	1.971	5	Pass	OK
1045	.738	.687	1.378	5	Pass	OK
1046	.352	.980	1.091	1	Pass	OK
1049	.612	.699	1.695	?	not cleaned	OK
1061	.193	.971	1.075	5	Pass	bridge

GSFC EVALUATION DATA USED TO IDENTIFY FIBER OPTIC CONNECTOR REPEATABILITY

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SMA style, single terminus, fiber optic connectors are used on GSFC hardware at box and transceiver interfaces. By virtue of its mechanical design, this type of connector has inherently lower connection repeatability when compared to more modern, single fiber connectors. This lack of repeatability can cause uncertainty when making loss measurements, especially when other components in the link are being held to tight tolerances (@ 0.1 dB).

The design of the coupling mechanism is a root cause of this lower repeatability. The SMA connector uses a threaded coupling nut with no keying device. Connector plugs are mated with an adapter which brings the fiber ends very close to each other without causing them to touch. This allows a small air gap between the fiber ends which typically accounts for the majority of loss for the connector pair. This loss will increase as the length of the air gap increases. The same air gap loss applies to a connection with an emitter or detector.

The quality of the coupling nut thread and the thread on the adapter has been found to cause variation in the size of the air gap between the glass interfaces. Though a torque value is specified by the manufacturer, burrs on the coupling nut threads, or adapter threads, can make the connector seem fully mated for several different axial positions. Low levels of vibration, such as is encountered during bench testing, can cause the coupling nut to loosen, allowing the connector to back off, increasing the air gap. Though a poor mating condition can exist at an active device, the connector-to-connector interface will suffer the most from an incomplete mate.

SMA's are "non-contact" connectors whose loss performance will always be limited by the presence of an air-gap. Modern connectors have been designed to eliminate the air-gap loss by incorporating specially polished termini that make physical contact with each other (PC). The termini in PC connections are spring-loaded to ensure that physical contact is made. The spring also protects the glass-to-glass interface from excess mating stress that could damage the fibers. ST, SC and FC style connectors which incorporate a single PC polished terminus, can be used as a form and fit replacement for the SMA connector, however they have not yet been fully qualified for use in GSFC flight hardware.

Optical throughput data, that can provide insight to SMA connection repeatability, was taken during the course of an evaluation of a multiple termini fiber optic connector for the GSFC Parts Branch (Code 311). A transceiver module with two emitters, each with a launch cable, was used to send light through a cable assembly consisting of cable sections terminated with SMA connectors. The multi-termini cable assembly consisted of four optical paths going through a miniature circular connector (MIL-C-38999, Series III type), each path consisting of two cable sections. Each of these cable sections had an SMA connector on one end and a MIL-T-29504 contact, with a PC polish, on the other end. The far end of the multi-termini cable assembly was directly connected to an optical-to-electrical (O/E) converter whose output was fed to an oscilloscope. Optical throughput was calculated from the mV value displayed on the oscilloscope.

The data was originally taken to characterize differences in data capture techniques and to baseline two SMA-to-SMA launch cables. Ten measurements were taken for each of the 32 launch/cable section/data capture configurations. By making and breaking the connections, between each measurement, 320 separate data points were established.

The data was analyzed to provide mean and standard deviation values for each sample. All aspects of the set-up were constant within a given data sample except the coupling efficiency between the launch cable and the input end of the multi-termini cable assembly. All of the SMA connectors were the same type. The connectors on the cable assembly were from the same production lot and the connectors on the launch cable were from the same production lot. All of the SMA connectors were terminated at the same time, under the same conditions. Combining the data taken for both emitters and both measurement techniques should impose a multimodal characteristic on the sampling distribution curves.

Statistics for the 32 samples are shown in Table 1. A quick review of the data in Table 1 shows that the Xbar and s values are very similar in magnitude. This allows one to use the statistics from each data set to obtain the graph shown in Figure 1.

Table 1. Statistics for 32 Samples of N=10

Sample	1	2	3	4	5	6	7	8
Mean (Xbar)	-9.584	-9.608	-9.371	-9.079	-9.784	-9.599	-9.440	-9.521
Standard Deviation (s)	0.272	0.213	0.321	0.269	0.171	0.177	0.474	0.145

Sample	9	10	11	12	13	14	15	16
Mean (Xbar)	-9.224	-9.684	-9.643	-9.180	-9.893	-9.503	-9.394	-9.250
Standard Deviation (s)	0.180	0.260	0.215	0.134	0.060	0.265	0.235	0.218

Sample	17	18	19	20	21	22	23	24
Mean (Xbar)	-9.445	-10.007	-9.579	-9.220	-9.665	-9.523	-9.462	-9.454
Standard Deviation (s)	0.224	1.431	0.284	0.158	0.203	0.239	0.359	0.137

Sample	25	26	27	28	29	30	31	32
Mean (Xbar)	-9.401	-9.684	-9.659	-9.474	-9.886	-9.405	-9.416	-9.253
Standard Deviation (s)	0.214	0.260	0.242	0.269	0.162	0.093	0.247	0.099

The mean and standard deviation values calculated for the 32 individual sample sets are very similar in magnitude allowing them to be graphed together.

Table 1 shows the sampling data of the means and standard deviations in the 32 data sets. When represented in graphical form, both populations are characterized by a normal distribution though the standard deviations curve does reflect the mixed variables in the original data. The mean and standard deviation statistics for the sampling distributions are shown in Table 2 below. The low value of 0.052 dB for s for the sampling distribution of the standard deviations allows one to estimate that a loss measurement taken for these SMA-to-SMA connections can deviate from its mean value by 0.179 dB to 0.335 dB without any real change in the physical condition or reliability of the connectors. In other words, the repeatability of the connection is between 0.179 dB and 0.335 dB with an average repeatability of 0.257 dB.

Table 2. Statistics for Sampling Distributions

Population	Xbar in dB (mean)	s in dB (standard deviation)
Means	-9.512	0.210
Standard Deviations	0.257	0.052

A typical connection repeatability value can be estimated using Xbar for the sampling distribution of the standard deviations of the 32 data sets.

In conclusion, this sample data roughly quantifies the repeatability of an SMA-to-SMA connection as around 0.257 dB. This does not mean that an SMA connection cannot be optimized for low loss (@ 0.1 dB) but it does add some uncertainty to delta calculations and baseline measurements that involve breaking an SMA connection (to access a power meter for example). Careful baselining for repeatability for all SMA connectors used in system hardware and in test set-ups should be standard laboratory practice. This type of baseline data will provide more confidence in measurements taken throughout an optical system's verification and qualification test cycle and will give the user a better understanding of loss budget tolerances.

HIGH DENSITY SPACEFLIGHT APPLICATION OF PEMS WITH PARYLENE CONFORMAL COATING

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Abstract

The approach used for the Spartan 207 at NASA's Goddard Space Flight Center is one solution to the long standing problem of using non hermetic devices in critical applications. Plastic Encapsulated Microcircuits (PEMs) have traditionally not been accepted as qualified for use in space flight applications. To remove these bariers, NASA/GSFC is using Parylene Coating on high density plastic packages for space flight application. In addition, numerous benefits have been found using a UV enhancer with the Parylene C over plastics for the Spartan 207 project. This paper discusses the use of plastics on the Spartan-207 mission which requires hardware to be re-used several times with on ground storage periods between uses. To meet the mission needs it was necessary to develop an approach that would enable the use of the plastic devices without the inherent increased risk normally associated with non hermetic devices. The use of UV enhanced Parylene C was found to be an approach that met all mission requirements.

Introduction

The Spartan 207 mission deploys an inflatable radio antenna during the May 1996 trip of the shuttle. The Spartan platform is deployed from the shuttle and inflates a mylar antenna to 100 feet in length and 50 feet in diameter. The reusable, free flying space platform will be retrieved after jettisoning the inflatable antenna and returned to the shuttle bay. The Spartan is basically a rectangular shaped box with experiments occupying about half the volume and the support systems occupying the rest. The support systems include Altitude Control, Data Handling and Storage, and Thermal Control. Unique to the Spartan "free-flyer" is the desire to reuse the platform. The platform with its support systems must be able to survive for an indefinite period in each of the following environments: manufacturing, long and short term ground storage, launch, and low earth orbit during deployment. In many ways this is a more strenuous requirement for plastics when compared to typical consumer use. Rather than use hermetic devices the desire was to use newer technology Flash EEPROMs available in a commercial plastic Thin Small Outline Package (TSOP) from Intel for the Solid State Recorder. The Spartan solid state recorder using plastic TSOPs was designed and manufactured by SEAKR Engineering, Incorporated, of Englewood, Colorado, with this desire in mind. The Spartan 207 solid state recorder contains up to 512 Mbytes of non-volatile memory using the Intel 32 Mbit Flash EEPROMs. Use of this off the shelf plastic device provides an inherant non-volatile, low power, cost-effective and high density solution for the high reliability application of the Spartan 207 platform.

Space and Ground Environment Limitations

The low earth orbit (an orbit around the earth at less than 1,000 kms) presents unique application requirements. The thermal concerns include both severe temperature cycling and steady state requirements. In addition mechanical concerns especially through launch include acceleration, vibration and shock. The environment presents requirements for control of outgassing, flammability, radiation tolerance, plasma effects and the ability to perform in zero gravity and zero pressure. Prior to launch in the manufacturing, storage and handling phases, the ingress of moisture becomes an added concern.[4] Moisture has been found to be one of the major components especially in conjunction with factors such as ionic contamination, voltage, temperature and time, that severely shorten the life expectancy of microcircuits. This has been well studied and documented and is obviously a greater issue with non hermetic devices. PEMs absorb moisture, even with the improved encapsulants available in the industry today. A good guideline for the maximum allowable moisture absorption is 0.11% by weight as a function of temperature and humidity. This amount can be reached in some cases in as little as 72 hours in an environment of 30°C at 70% relative humidity.[9] Moisture absorption is much faster on PEMs with manufacturing or design defects, even in low humidity conditions. "Ruggedizing" these parts by adding a hydrophobic coating is a practical, viable solution. Goddard Space Flight Center chose Parylene C for just this application.

Parylene C over Plastic

Parylene as a coating has been found to effectively lengthen the life of components that have been tested through strenuous temperature, humidity and bias conditions. Although the material is not hermetic, the

hydrophobic properties (water absorption at less than .1%) have been found to be very effective as a barrier. In one study, after 1,000 temperature cycles of-55 °C to 85°C non coated ceramic and plastic devices were nearing the end of their useful life. By contrast, the parylene coated boards had significant useful life remaining.[2] Parylene is an effective barrier to oxygen, moisture, and carbon dioxide, which is directly related to extended solder life in the interconnects.[9] The ability of Parylene to coat without forming thick fillets which can lead to high stresses and sites of crack initiation during manufacturing and assembly processing has been known for years.[5]

Parylene C was selected due the following factors:
a) It is chemically stable, relatively inert with an absence of trace contaminants and meets NASA's low outgassing requirements.[1][6]

b) It is mechanically stable between -200 °C and 150°C with excellent adhesion properties.[9]

c) It is a low stress coating that does not form sites prone to crack initiation by conforming to the entire topography of the board and parts[7], and has low or minimal impact of package cooling.

d) Parylene's hydrophobic nature makes it a significant barrier to penetration of ionic or moisture species even at thicknesses less than 0.025mm.[10]

e) Protects assemblies from surface contamination, process dust, chemicals, mechanical damage and corrosion[10].

f) Parylene C exhibits a useful combination of electrical and physical properties such as high dielectric resistance(MIL-I-46058 compliant).

g) If necessary, parylene can be removed by heating, abrasion, or micro-abrasive blasting.

h) Parylene C has a coefficient of thermal expansion (CTE) highly compatible with plastic encapsulant materials.

Typical properties of Parylene C are given in Figure one[10].

Parylene Application

In the Parylene process, after proper cleaning, the assemblies are placed in the deposition chamber and will remain at room temperature during the coating process. The crystalline solid dimer, di-p-xylene is sublimed under vacuum at 175 °C and then pyrolized at 680 °C to produce the reactive intermediate p- xylene. The monomer spontaneously polymerizes on surfaces in the vacuum of the sample chamber to produce a continuous film of linear poly(p-xylene). The entire process takes place in three significant stages on a standard coating machine.
First, the dimer is carried into the pyrolysis chamber by reduced pressure there. The dimer is cleaved in the pyrolysis chamber, and then moves as a vapor into the sample chamber. In the sample chamber, a short mean free path of the molecule vapor, less than 1 mm, assures a slow forming uniform coating. Additional annealing steps can be added to increase the hardness of the parylene coating.

Figure two[7] graphically describes the parylene C coating process.

Status of the Spartan Boards

Six boards were coated for the Spartan 207 project by NASA/GSFC's Materials Branch using a parylene vapor deposition system. Four of the boards are part of the Spartan's data recorder. Two of these boards are populated with plastic Thin Small Outline Packages (TSOPs). The boards were thoroughly cleaned in accordance with NASA standards to improve adhesion prior to the coating process. The pre coated board cleanliness is a significant issue. Flux and contaminant residue left on a board under Parylene coating could potentially develop corrosion, vesication, blistering, electromigration or other stresses leading to long term coating adhesion problems.[8] Prior to the deposition of parylene on two of the boards, a fluorescing material, Calcofluor, was added to the pre-deposition parylene powder. This material disperses evenly along with the Parylene during the deposition process and helps in detecting flaws in the coating. No flaws were found during visual exam under magnification after coating the assemblies. Using the three step deposition process, a one mil. (0.025mm) layer of parylene "C" was deposited on the surface of the boards. The coating thickness was verified visually using a one mil. aluminum foils. Parylene film has been found to meet all coating protection electrical insulation specifications (MIL-I-46058) as thin as 0.5 mil (0.012mm).[8] Typical application thickness ranges from a few hundred angstrom to three mils. The 1 mil. (0.0025mm) application we chose through process proofing is well above the minimum thickness requirements. Throughout the procedure, the boards continually remain at room temperature inside the deposition chamber.

As part of the flight qualification process, environmental testing of the assemblies will be performed to simulate actual flight and ground conditions.

Findings

The benefits found from the Spartan 207 approach included the ability to maximize visual inspection ability with a thin, clear, transparent coating. By enhancing the Parylene with the UV visible material the ability to visual inspect the coating for defects in the material such as pitting or lack of coverage is also easily attainable. The increased hydrophobic properties of the assembly protect from the moisture ingress normally associated with ground processing and storage. Low outgassing materials such as Parylene are mandatory for critical applications in space. Outgassed materials are detrimental to the instruments and operational components of a spacecraft and in particular any optics. The most important benefit of the parylene coating is the ability to use the best devices available for the application. In this case the Flash EEPROMs available from Intel as 'off the shelf, commercially available' in a non hermetic package avoided the use of traditional, custom and costly devices which would not fit the application as well.

Summary

The approach of using a UV enhanced Parylene over plastic devices has many benefits for critical applications. With this approach there is the ability to select from a wider range of device types available. Besides the greater availability, there is also the ability to use newer technology chips that are not marketed in traditional hermetic packages. The use of the lighter, more dense plastic packages allows for the decrease in size, weight and volume, while increasing functionality. Parylene C is not the ideal material for every application. Parylene is more costly to apply than the traditional conformal coats used by the space industry, primarily uralane type coats, and more difficult to remove. For the Main Electronic Box on Spartan 207, Parylene C was chosen to coat hermetic devices primarily for its improved resitivity. The Indian Space Agency (the 6th largest space agency in the world) uses Parylene exclusively and with major success in all applications.[3] The use of Parylene C can be defined as an enabling technology opening the door to a much greater use of plastic components in critical applications.

Additional Programs

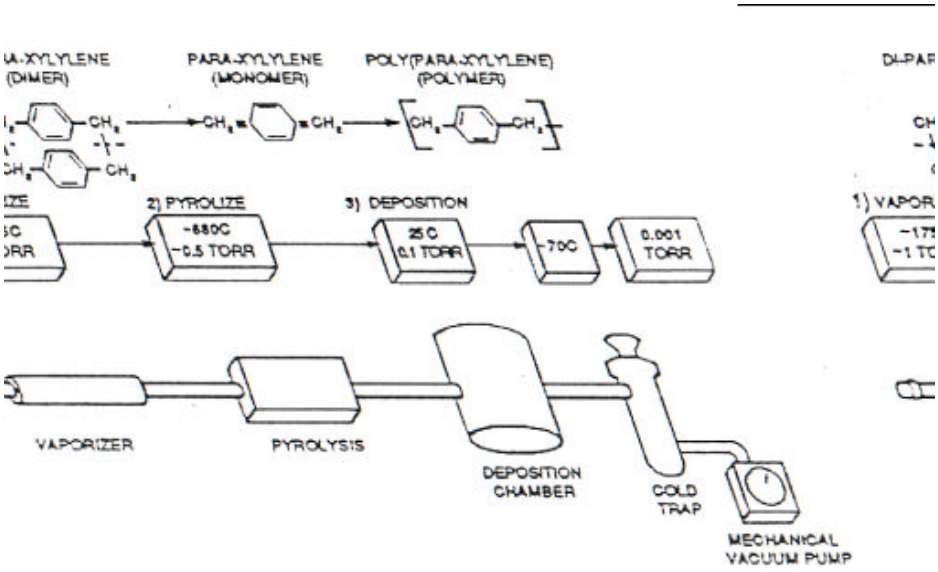
NASA/GSFC is currently exploring the possibility of extensive use of high density plastics (stacked TSOPs) coated with parylene C and Calcofluor for several future programs. The use of Stacked TSOPs for large scale Dynamic RAM memories has been chosen for the EOS-AM mission. The use of Parylene C over bare chips is being studied in a consortium agreement with the Johns Hopkins Applied Physics Lab, and the GSFC Assurance Technology division is just completing a study of coatings and interconnects over stacked die. Additional testing of Parylene "C" with the Calcofluor additive as a viable coating solution with respect to NASA's materials requirements is also planned. Special appreciation goes to Mark Steiner, Dennis Olivares, the Spartan 207 Project, Carroll Clatterbuck our GSFC Parylene expert, and SEAKR Engineering, Inc.

Figure 1: Typical Engineering Properties of Parylene C

Property	Parylene C	ASTM method
General		
density, g/cm^3	1.289	D1505
refractive index, n_D^{23}	1.639	
Mechanical		
tensile modulus, GPa[a]	3.2	D882
tensile strength, MPa[b]	70	D882
yield strenght, MPa[b]	55	D882
elongation to break, %	200	D882
yield elongation, %	2.9	D882
Rockwell hardness	R80	D785
coefficient of friction		
static	0.29	
dynamic	0.29	
Thermal		
melting point, °C	290	
linear coefficient of expansion at 25°C, J/(gK)[c]	3.5	
heat capacity at 25°C	1.0[e]	
thermal conductivity at 25°C, W/m(K)	8.2[e]	
Electrical		
dielectric constant		D150
60Hz	3.15	
1kHz	3.10	
1MHz	2.95	
dissipation factor		D150
60Hz	0.020	
1kHz	0.019	

1MHz	0.013	
dielectric strength at 25µm, short time, MV/m	220	D149
dielectric strength at 25µm, step-by-step, MV/m	185	D149
volume resistivity at 23°C, 50% rh, Ω	$8.8x10^{16}$	D257
surface resistivity at 23°C, 50% rh, Ω	$1x10^{14}$	D257
Barrier		
water absorption, %	<0.1	D570
water vapor transmission at 37°C ng/(Pasm)[g]	0.0004	E96
gas permeability at 25°C, amol/(Pasm)[g]		D1434
N_2	2.0	
O_2	14.4	
CO_2	15.4	
H_2S	26.0	
SO_2	22.0	
Cl_2	0.7	

Figure 2: Parylene Coating Process



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PROGRAMMABLE LOGIC APPLICATION NOTES

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This column will be provided each quarter as a source for reliability, radiation results, NASA capabilities, and other information on programmable logic devices and related applications. This quarter the focus is on Actel/Loral Radiation-Hardened Field Programmable Gate Arrays, the initial SEE evaluation of the Act 3 A1460A device and some design tips. Next quarter, radiation-hardened PALs will be discussed, results of a SEE test on Quicklogic FPGAs, and some more design tips. If you have information that you would like to submit or an area you would like discussed or researched, please give me a call or e-mail.

ACTEL/LORAL FPGAs

The Air Force/Phillips Laboratory is funding development of radiation-hardened Field Programmable Gate Arrays (FPGAs). This note will describe some of the technical aspects of the developments and current results.

DEVICES: The RH1020 and the RH1280 are radiation hardened versions of the A1020B (1.0 µm) and the A1280XL (0.8 µm) and are functionally compatible. Principally, the A1020B has improved clock skew performance over its predecessors. Here is a brief list of differences for the A1020B: (1) Increased drive and speed for the clock network by use of an independent, enlarged, TTL translator at pad; (2) high-efficiency buffers for the clock tree; (3) row drivers for clock shorted together behind the isolation device for current sharing; and (4) widening of the isolation device which lowers series resistance at the top of the clock tree for smaller propagation delays and reduced skew. The A1280XL differs from it's predecessors (such as the A1280A) in the following ways: (1) I/O modules are redesigned to improve pin-to-pin and clock-to-output delays; (2) enhanced clock trees minimize clock delays and skew; (3) different characteristics for SDI and DCLK when unused [see last quarters notes]; and (4) the A1280XL has a slightly different specification for the programmer/debugger, with three more bits in the command shift register than the A1280A.

SPECIFICATION: The RH1280 will be added to 5962-90156 (submittal end of March) and the RH1020 will be added to 5962-90965 (submittal end of Q2).

FOUNDRY AND PROCESS: All manufacturing operations including device fabrication, assembly, and test will be done at Loral with parts built on their radiation-hardened epitaxial bulk RHCMOS process (0.8 µm). The base layers are standard Loral process with high voltage transistors and ONO antifuses Actel designs. The thickness of the antifuse has been increased to prevent Single Event Dielectric Rupture (SEDR), a partial programming of an antifuse by a heavy ion. Nominal Actel antifuse thickness is ~ 86Å (oxide-equivalent) and the RH1280 lot currently in qualification is using a 99Å thick antifuse. Use of the Loral plug technology ensures no step coverage issues with these parts. The parts will be run on a 5V line; 3.3V parts, if available, will be a characterized version of the 5V parts as there is no plan to move to the 3V line.

PACKAGES: Standard packages will be the QFP172 for the RH1280 and the QFP84 for the RH1020. PGAs will be a special order. All lids will be grounded (current Actel products have floating lids).

TIMING PERFORMANCE: For the RH1280, a pre-radiation timing model is available for Designer 3.0 by installing the 3.0.1s silicon update and post-300 krad model will be available in Designer 3.1 No estimate for performance of the RH1020 has been received.

PROGRAMMING: Programming will be supported on the Activator 2 and the Activator 2S starting with Designer 3.1. Data I/O programmers will not be supported for either of the devices. Programming yield is expected to equal that of standard Actel devices and Actel's return policy for devices that do not program will be maintained. Because of the increased thickness of the antifuse, programming time per device will substantially increase, with current patterns taking approximately 50 minutes per device.

RADIATION PERFORMANCE (RH1280):

TOTAL DOSE: Approximate 10% increase in t_{pd} @ 300 krads. I_{cc} information not yet available. Gross functional failure started to occur at 500 krads, with V_{CC} = 4.5 VDC.

SEU: Single Event Upset performance of C- and S-modules shows similar results to the A1280A. This extends to error rates and the sensitivity to logic state. SEU performance of the I/O latches has not yet been measured and will be tested in the near term.

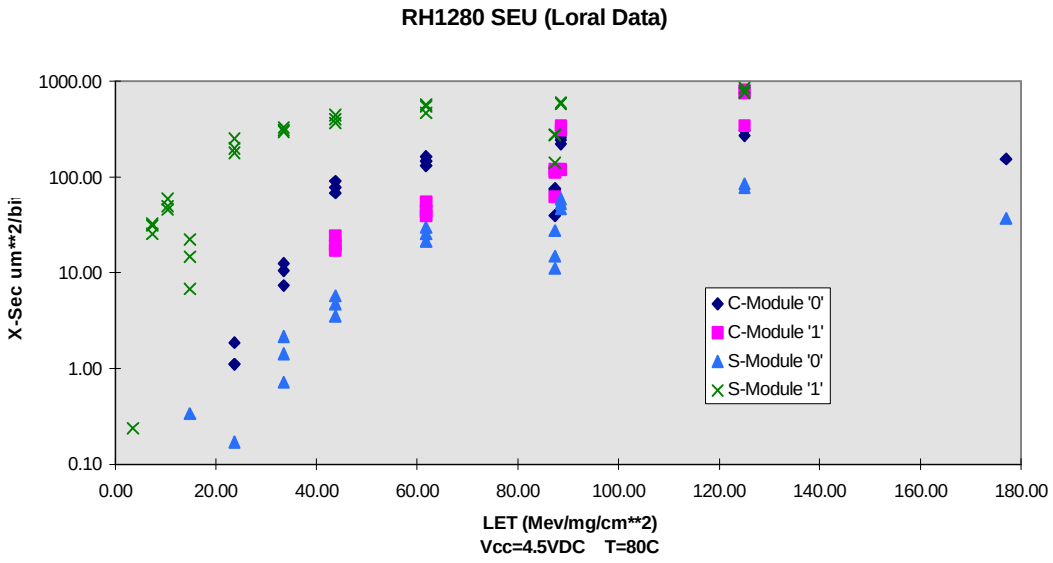
SEDR: With the increase of antifuse thickness, it is expected that no Single Event Dielectric Rupture (antifuse partial programming by a heavy ion) will occur. Test results to date have detected no SEDR.

LATCHUP: The devices are expected to be latchup immune. Tests showed no latchup at an LET of 180 MeV-cm ^{2}/mg at V_{CC} = 5.5 VDC at a temperature of 125°C.

DOSE RATE UPSET: > 1 x 10^9 rad(Si)/sec (target).

SURVIVABILITY: > 1 x 10^{12} rad(Si)/sec (target)

NEUTRON FLUENCE: > 1 x 10^{14} N/cm^2 (target)



DESIGN TIPS

(SEE PERFORMANCE OF ACTELFPGAs)

Flight applications of FPGAs are increasing with more designers starting to utilize these devices. Additionally, high level design tools, such as macro generators, optimizers, and hardware description languages provide a level of abstraction to the designer. However, to ensure successful on-orbit performance and meet mission requirements, it is necessary to understand the underlying implementation and the radiation effects. Recently, an application with significant SEU requirements (LET threshold of 37) was designed using high-level tools, with the designer unaware of the Actel FPGA architecture and implementation dependent radiation susceptibilities which resulted in late design modifications (unpleasant at that stage of the project). This tip shall review storage elements in the Actel FPGAs and SEE data for each of the products and structures and the implications of using advanced tools.

There are currently 4 basic families of Actel FPGAs: Act 1, Act 2 (and A1200XL), Act 3, and the 3200DX. The Act 1 devices are composed entirely of C-Modules (or combinational modules) and I/O modules. Both of these modules are purely combinational and have no storage capability. Flip-flops are made by configuring a single C-Module as a transparent latch or by using two C-Modules as an edge-triggered flip-flop. The Act 2 family added the S-Module (essentially a C-Module followed by a dedicated flip-flop) and transparent latches to the input and output paths in the I/O modules. The S-Module flip-flop may be configured as either an edge-triggered device or a transparent latch. The Act 3 series replaced transparent latches in the I/O modules with edge-triggered flip-flops driven by a high performance clock that guarantees a t_h of 0 nS for input flip-flops. For storage, the 3200DX family adds internal dual-port SRAM to the Act 2 resources. To date, the A1020x (Act 1) and the A1280x (Act 2) have been subject to significant SEE studies. The A1460A (Act 3) and the RH1280 have been subject to initial tests, with the A12xxXL and the RH1020 planned for testing in the near future. Planning has started for testing the A32200DX (20,000 gate array, internal SRAM, and JTAG). The following table summarizes SEE performance (and will be updated as new results come in):

Device	Feature Size	SEU Let th	Sat x-section	Temp
A1010	2.0	25	$5x10^{-6}$	R-->100C
A1020	2.0	25	$5x10^{-6}$	R-->100C
A1020A	1.2	25	$3x10^{-6}$	R
A1280 C	1.2	23	$3x10^{-6}$	R-->100C
A1280 S	1.2	5	$8x10^{-6}$	R-->100C
A1020B	1.0	28	$2x10^{-6}$	R
A1280A C	1.0	28	$2x10^{-6}$	R
A1280A S	1.0	5	$8x10^{-6}$	R
A1280A I/O In	1.0			
A1280A I/O Out	1.0	28		
A1280A 3.6V	1.0			R
RH1280 C	0.8	22	$8x10^{-6}$	R-->125C
RH1280 S	0.8	3	$9x10^{-6}$	R-->125C
RH1280 I/O In	0.8			
RH1280 I/O Out	0.8			
A1460A C	0.8		$\sim 2x10^{-7}$	R
A1460A S	0.8	>6	$1x10^{-6}$	R
A1460A I/O	0.8			
A1460A C 3.3V	0.8	~25	$8x10^{-7}$	R
A1460A S 3.3V	0.8	<6	$2x10^{-6}$	R
A1460A I/O 3.3	0.8			

Device	Feature Size	SEL	SEDR	Clock Upset
A1010	2.0	NO		
A1020	2.0	NO	YES	Observed
A1020A	1.2	NO	YES	
A1020B	1.0	YES*	YES	
A1280	1.2	NO	YES	
A1280A	1.0	YES†	YES	
A1280A3.6VDC	1.0	NO	NO	
RH1280	0.8	NO	NO	
A1460A	0.8	NO	YES	

NOTES:

1. A1460A Results same for routed global clocks and HCLK.
2. * Latchup for A1020B detected at LET = 55 MeV/(mg/cm^2)
3. † Latchup detected only with MODE pin high.
4. Single cell, C-Module latches have not yet been tested. A1020B tests planned in near term.
5. Blank cells denote either 'not measured' or 'not yet observed.'
6. Cross-sections are in cm^2/flip-flop

THE OBVIOUS CONCLUSIONS ARE:

1. Flip-flops made from two C-modules are relatively hard.
2. Flip-flops made from a single S-Module are relatively soft.
3. TMR techniques are required to make flip-flops very hard ($< 10^{-10}$ errors/bit-day)
4. A1020B devices are the only devices known to latch up.
5. All devices tested, with the exception of the RH1280 (preliminary tests), have shown susceptibility to SEDR. This is expected, since all of the devices share a common antifuse design. Running at 3.6 VDC lowers the bias across the antifuse and no SEDR was observed under these conditions.
6. RH1280 devices offer no significant improvement in SEU performance for C- and S-Modules.
7. 3.3 volt operation eliminates SEDR from Actels and increases SEU rate.

Now, commercial optimization and design tools tend to provide efficient commercial designs; that is, they will fit the logic compactly in a fast implementation. The major implication is that flip-flops are most efficiently implemented by using a S-Module (non-Act 1 designs) where a logic function can often be combined in the same module for no increase in resources and with no speed penalty. However, as was the case in one application, the SEU performance was substantially degraded, resulting in a redesign.

PROGRAMMING TIPS

1. When using Windows for Workgroups 3.11, it is recommended that the network connection be removed prior to programming devices. It has been noted that certain network disruptions can cause the PC to hang.

2. Uninterruptible Power Supplies (UPS) should be used when programming RH1280 devices. This is recommended based on the increased programming time and high cost of the devices.

3. For users programming Act 1 devices in the ALS 2.3.1 or 2.3.2 systems, there is a bug in the programming algorithm which may result in incorrectly programmed devices. There is a patch available to fix this bug.

4. On Act 3 devices, the HCLK and IOCLK nets cannot be internally probed in Debug.

5. There are no adjustments to be made on the Activator programmers. However, there is a calibration procedure which should be run periodically to ensure that the programmer is operating within specification. The procedure is available on Action Fax, uses standard laboratory equipment, and takes approximately 1/2 hour to run. Currently, our lab runs the calibration procedure every 6 months or after shipment of the hardware prior to programming flight parts.

6. Statistics should be kept on programming yield (at least informally). An abnormally low yield on semi-custom packaged devices led to the finding of inadequate device preparation and the need for corrective action. Normally, we have seen yields of 98% or higher.

SOCKET TIPS

The Actel 1995 Data Book recommends the Yamaichi socket for the A1280 in a CQFP172 package. However, this socket will only work on parts with date codes later than 9502. To be compatible with older parts that may still be in stock, use the Enplas OTQ-196-0.635-04, which is similar to the socket on the Activator programmer adapter.

ACT 3 EVALUATION

A joint effort by NASA (GSFC and JPL) and Aerospace Corp. is underway to evaluate the Act 3 family in the radiation environment. All testing planned will be conducted on the Actel A1460A (Matsushita die) in either a 207-pin PGA or a 196-pin QFP. The TD1460 design, based on the TD1020 and TD1280, will be used for total dose testing with a Cobalt-60 source. The RK3, based on the TMRA1BRB and TMRA2.C (GSFC designs) and the AERO1020 and AERO1280 (Aerospace designs) will be used for SEE testing. Additionally, 5 RK3's will be instrumented and flown in a space-borne experiment to compare on-orbit performance with predictions from ground-based testing. The A1460A consists of the equivalent of approximately 6,000 gate array gates and is a 0.8 µm part. While the A14100 10,000 gate part is more attractive for flight applications, the A1460A was furthest along on product development by Actel and was available for testing.

In the Act 3, we will be testing some new architectural features. I/O modules have edge-triggered flip-flops, with the input registers attractive for system designs with the 0 nS hold time specification. Also, there is a new internal high-speed clock, the HCLK. Registers are made utilizing these new features in addition to shift registers made from C-Modules, S-Modules, and a TMR string made from S-Modules. Some new features are included in this chip to improve SEE testing. The logic can directly look at combinational and clock upsets, based on clock upsets observed on the A1020x series. Also, the TMR string has been upgraded for the maximum protection against SEU's. First, the number of voting circuits has been tripled- this ELIMINATES the overhead and speed penalty for discrete voters since the 4:1 mux which implements it is combinable with the flip-flop receiving 'corrected' data. Also, a combinational upset on a voter would be ignored since the voters themselves are all redundant. Now a TMR flip-flop consists of just 3 S-Modules for these shift registers. While this scheme has the desirable features listed above, it does place a greater load on the internal routing resources. It turns out that it was fairly easy to place the three flip-flops in a triplet in very close proximity to each

other and the circuit routed with no problems. Additionally, timing analysis showed that the circuits, with test logic, will operate at 40 MHz internally, at worst-case conditions.

The RK3 test chip consists of 4 different modes: Johnson twisted ring counter; direct inputs allowing any waveform to be entered; stream of 1's, and a stream of 0's. The 0 and 1 streams are useful for determining upset rates as a function of state, the direct input is useful for chip failure diagnostics as well as arbitrary pattern input, and the Johnson twisted ring counter is directly compatible with previous AEROxxxx designs and test equipment and gives an average upset rates for the two states.

There are 500 flip-flops in shift registers in the RK3, divided as follows:

MA1, MA2: 50 C-Modules using routed clock.

MB1, MB2: 50 S-Modules using HCLK.

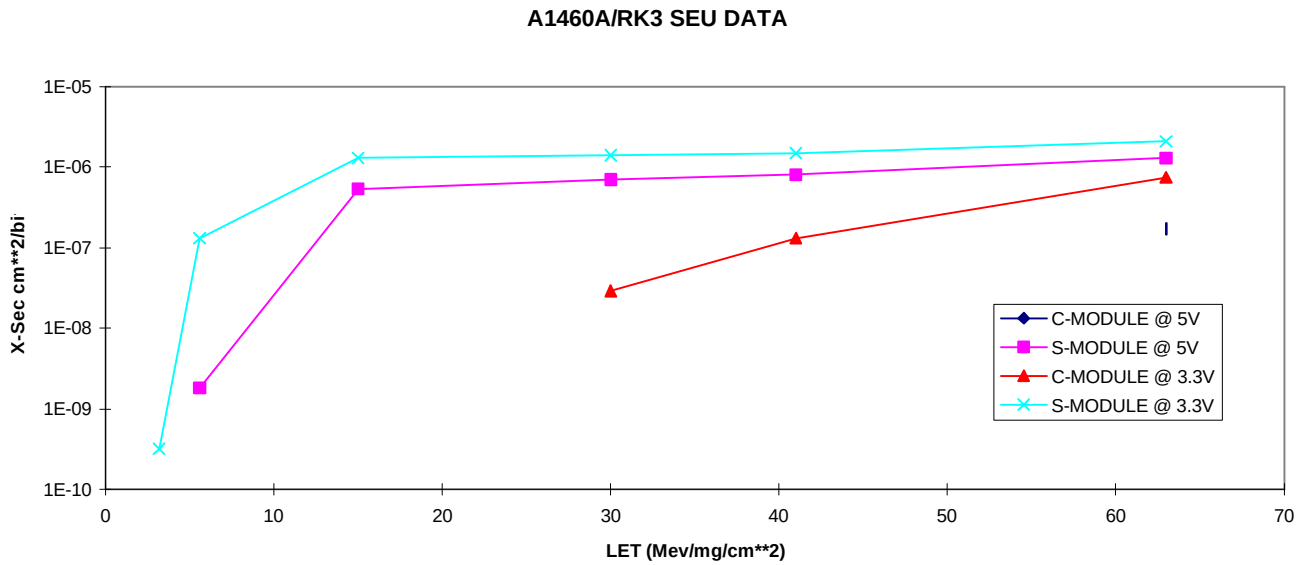
MB3, MB4: 50 S-Modules using routed clock.

MC1: 50 TMR-Modules using HCLK.

I/O: 50 Input Flip-flops (IREC) using IOCLK.

SEE test goals, in addition to standard SEU rates, SEL and SEDR detection, etc., include characterization at 3.3 VDC. The flight experiment will be in-flight configurable for either 3.3 VDC or 5.0 VDC bias. Total dose tests have been run on TD1020 and TD1280 devices over a range of bias voltages and a comparison will be made between families.

Preliminary SEE testing of the RK3 A1460A has been completed. Key parameters are included in the above table and data is shown in the chart below. No latchup was detected and as with other dielectric antifuse devices, SEDR was detected with heavy ions. Also, as expected, the SEU rate increased with decreasing supply voltage although no significant difference was observed when switching between 5.0 VDC and 5.5 VDC. As had been seen on A1280A's and more recently the RH1280, there was a SEU sensitivity to flip-flop state. The TD1460 device has been prepared and the bias board completed. A first look at the total dose performance is expected by the next edition of EEE Links.



ACKNOWLEDGMENTS and REFERENCES

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RADIATION TOLERANT PROGRAM MEETING JANUARY 23, 1996

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The following is a summary of the Radiation Tolerant program held at NASA Headquarters on January 23, 1996. The motivation of the program is to utilize the expertise of NASA, DoD, commercial satellite suppliers, VLSI industry and academia to develop a commercial basis to provide radiation tolerant VLSI to the nation. The goal of the Radiation Tolerant program is to develop a commercial source for radiation tolerant VLSI that has the following features:

- VLSI fabrication in commercial foundries using modern CMOS processes advanced by the electronics industry.
- Item Establishment of a commercial based radiation tolerant standard cell library.
- VLSI design is accomplished with popular, open commercial CAD tools used by the IC industry.
- NASA approved qualification path from wafers to packaged chips.
- Testing and validation of radiation tolerant VLSI.
- Commercial marketing and support of radiation tolerant standard cell library.
- Radiation tolerant standard cell library available to every commercial and Government VLSI design facilities.

The program partners are:

1. The NASA Institute of Advance Microelectronics at the University of New Mexico.
2. TRW Space and Electronics Group
3. The Aerospace Corporation
4. Compass Design Automation
5. Goddard Space Flight Center
6. Jet Propulsion Laboratory
7. Johnson Manned Space Flight Center

The strength and interest of each member is:

- The University of New Mexico (UNM) will serve as overall coordinator of the program. (UNM) provides basic SEU and SEL radiation tolerant technology and knowledge base for implementation.
- Aerospace Corporation has a history of DoD VLSI radiation hard expertise including total dose effects. A complete radiation and reliability research laboratory is available to qualify the radiation tolerant VLSI. This program is consistent with a major IR&D program launched by Aerospace towards providing radiation tolerant electronics to DoD for the future benefit of the nation.
- TRW is a major spacecraft designer with a goal of producing high performance, low-cost spacecraft of the future. A key element in the future development of space craft is access to modern VLSI technology to meet the computing requirements of the future. Moreover, TRW is a key member of the NASA New Millennium program.
- Goddard Space Flight Center is a major design center for NASA spacecraft. The GSFC interest is to develop a new source of VLSI circuits that are based on commercial foundries that make the design of next generation VLSI readily available for its missions. GSFC will be responsible to provide a qualification path for next generation VLSI.
- Compass Automation is the world's leading supplier of standard cell libraries and a leading VLSI CAD tool supplier. Compass has a commercial standard cell library that is used by a large number of companies throughout the world. The intent is to:
    1. Implement and maintain a standard cell library with radiation tolerant VLSI.
    2. Market and sell to spacecraft designers everywhere.

Conclusion

The radiation tolerant program appears to present a great deal of potential towards providing high performance electronics for the Space program. The team assembled for this program includes the elements to be successful: New radiation tolerant technology (UNM), radiation hard expertise and testing (Aerospace), user push to develop high performance VLSI (TRW and GSFC), NASA qualification and procurement expertise (GSFC) and the commercial outreach with an established standard cell produce that interfaces with common CAD tools (Compass). Plans are underway to create a radiation tolerant library that will be available in one year.

LINKING TO *EEE LINKS* ON THE WORLD WIDE WEB

Web Page Capabilities

by Doug Smith
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Have you seen Web pages that display multiple HTML documents at one time? This is a recent capability of some Web browsers. An HTML programmer can display different HTML documents, each in its own 'frame'. For a user to see the frames, he or she needs a frames-capable browser, such as Netscape 2.0. However, the documents can be set up so that they will display in other browsers even though the frames will not be there.

Frames provide the capability to have a table of contents permanently displayed on part of the browser window, and allow the user to view the document sections in the rest of the window. If a document section has a link to a picture, the picture could then be displayed in a third part of the window. Each different part of the browser window is called a frame. Check out the October 1995 issue of EEE Links to see an example of using frames.

As the World Wide Web becomes more and more a part of our everyday lives, businesses are also moving to the use of Web interactive databases. Having a Web interactive database of a company's employees would allow personnel data to be maintained from around the world without any concern for the type of computer systems the users have. These Web interactive databases can also be developed on almost any platform and use almost any existing database application.

For government employees and contractors, the EEE Parts Information Management System (EPIMS) and NASA Alert Reporting System (NARS) are presently being migrated to a Web interactive platform (EPIMS-Web). This will overcome the present system's limitation of the required X-Windows platform, as well as speed up the retrieval of information significantly. With just an ordinary Web browser, the EPIMS-Web pages will look like a typical database interface, and users will be able to access all the same functions that were in previous versions of EPIMS.

Expect to see more and more of these and other capabilities in the future. For more information on HTML programming, developing Web interactive databases, or the EPIMS-Web task contact Doug Smith.

OUTGASSING PROPERTIES OF PEMS

by Robert Savage,
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The Electronic Packaging and Processes Branch, Code 312, has recently completed a study characterizing the outgassing properties of plastic encapsulated microcircuits (PEMs). The report details the evaluation of a total of 21 PEMs in a variety of package styles from twelve different manufacturers. The data showed a wide variation among manufacturers and various package styles attributable to the differences in the formulation of plastic molding compounds used. The experimental results clearly demonstrated that there outgassing results were well below the 1.0 percent total mass loss (TML) and 0.1 percent collected volatile condensable material (CVCM) requirements for space flight use.

However, as seen from this study, it is important to realize that significant variability was seen in the outgassing characteristics of a small sample of plastic encapsulated microcircuits. Under normal manufacturing conditions, significant variations may be expected across a range of products and among manufacturers. This is expected due to the differences in the material formulations and manufacturing processes among various manufacturers.

No attempt was made in this study to characterize physical or chemical properties of molding compounds or evaluate the effects of long term storage environment and correlate those with the outgassing characteristics of plastic encapsulated microcircuits. The effects of the parameters such as moisture content in the molding compound, storage conditions etc., should be studied in correlation with corresponding outgassing data of the encapsulating materials to address the suitability of plastic encapsulated microcircuits in space flight applications.

For further information or a copy of the final report please contact Mr. Nitin Parekh at 731-8677 or Mr. Robert Savage at 286-9309.

CRITICAL ISSUES FOR RELIABLE APPLICATION OF PLASTIC ENCAPSULATED MICROCIRCUITS IN SATELLITES

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The following is an abstract from a paper presented by Nick Virmani at NEPCON West '96 in Anaheim CA Feb 26 - 29. For a copy of the paper please contact Nick Virmani.

The use of Plastic Encapsulated Microcircuits (PEMs) in space flight applications is becoming an increasingly important issue. PEMs are reputed to offer significant cost, availability, size and weight advantages over the hermetic devices in many space applications. On the other hand, PEM opponents maintain that, despite marked improvements in PEM construction techniques and in associated reliability data, there still is insufficient high reliability data to support their use.

Currently, there are no standard PEM processing, test, and qualification requirements which can be confidently used for space-level procurement. It is recognized that some JEDEC standards, covering test methods and procedures for PEMs, have recently been released by the Electronics Industry Association (EIA) and others have been proposed. It is also recognized that MIL-PRF-38535 has identified the necessary criteria to allow a PEM manufacturer to be included in the Qualified Manufacturers Listing (QML) and that some candidate QML PEM manufacturers have already been audited. However, the fact remains that the space community has not adopted any standards for PEMs; nor has it identified any requirements for PEMs to be used in space applications. This paper presents the critical issues related to the use of PEMs for space flight applications.

RELIABILITY CONCERNS FOR SURFACE MOUNT SOCKETS: ABSTRACT

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The following is an abstract from a paper presented by Robert Savage at NEPCON West '96 in Anaheim CA Feb 26 - 29. For a copy of the paper please contact Nick Virmani.

The use of through-hole devices, such as EEPROMs, which need to be removed and reprogrammed on surface mount boards presents a unique packaging problem. Traditionally through-hole mounted sockets have been used which allow for the removal, reprogramming, and replacement of these programmable devices. Surface mount boards take advantage of the ability to increase trace densities on inner layers to increase packaging density. The use of traditional through-hole sockets would therefore decrease this advantage in packaging density. Surface mount sockets were tested by the Electronics Packaging and Processes Branch at NASA's Goddard Space Flight Center utilizing testing equipment in the Assurance Technologies Lab. Results of this testing show reason for concern in the manufacturing process, use environment and lead configuration of part used. Manufacturing concerns include the lack of standard pad sizes and configurations for reliable connections. Lack of manufacturing process control could lead to solder starved connections, misalignment of socket placement, and poor wetting of socket solder connection. Part lead configuration and preparation could lead to solder joint cracking during on orbit thermal cycling. Finally, the number of insertions and extractions significantly affect the retention force of the sockets themselves. For these reasons, NASA's Goddard Space flight Center does not recommend the use of surface mount sockets without significant process controls and mission life qualification.

THE COSMIC RAY UPSET EXPERIMENT (CRUX)

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INTRODUCTION

When a single energetic, charged , elemental particle in space, (commonly called an ion or cosmic ray) passes through a microcircuit in an electronic system of a spacecraft, it deposits energy in to that chip. How much energy is deposited and how much charge is generated thereby is dependent primarily on the particle's atomic number and its energy. If the region where this charge was generated is collected in a "sensitive volume" of an electronic circuit, the circuit may malfunction . For example, in a memory cell of a RAM (Random Access Memory) chip, the charge collected by a sensitive volume could cause that cell to change logic state. In critical systems, such as attitude control or pyrotechnic applications, this could have dire results. In this example, there is no temporary or permanent damage to the cell or to the chip itself. The cell only knows that it has been "upset" and in effect reprogrammed (although inadvertently), and operates normally thereafter. There can also be other, rarer effects which can temporally or permanently damage the device. An example of this is latchup, for which the sensitive volume site is different from that for upsets, and which can cause uncontro lled currents and device burn-out.

All types of such errors are called Single Event Effects (SEE), since they occur due to the passage of a single particle through a chip. The problem has been recognized since the mid -70's, and in 1979 started to draw considerable attention. Many DoD and NASA spacecraft sustained upsets which required operational "work-arounds". The TDRS and Space Telescope are two examples. Some microcircuit types are very sensitive, others are not. To enable the assessment of how susceptible a part type might be, analytical models were developed which presumed to predict how many upsets would be experienced by a part type in a prescribed orbit. These models utilize ground test data obtained on part types at high energy cyclotrons and accelerators, together with accepted modeling of the radiation environment. The resultant upset rate thus generated is then given to system and project managers to enable decisions on corrective or circumvention actions, some of which can be expensive if deemed necessary for mission success. A problem in this is that no one really knew how accurate or inaccurate the model predictions were. Being within a factor of two or three would be quite acceptable, but errors of 10X or 100X , either over or under, are unacceptable.

EXPERIMENT PURPOSE

The purpose of the CRUX experiment was to try to validate the prediction models by flying test devices and comparing actual flight upset rates with predicted rates. Close agreement would assure confidence in the accuracy of the models, while large disagreement would indicate that the models needed additional work and revision. The selection of part types to serve as the Devices Under Test (DUTs) was based on their popularity with designers at Goddard and other NASA centers. What will be summarized here are the results of the sixth CRUX mission, which flew on the Air Force free-flyer satellite APEX (Advanced Photovoltaic and Electronics Experiment). The previous five CRUX missions, starting in 1983, tested other, different part types and all flew on Space Shuttle flights. Results (that is, upsets) on all these were either nil or meager at best, mainly due to the relative insensitivity of older part types and to the benign nature of the radiation environment of shuttle flights.

APEX MISSION

The APEX spacecraft is the instrumented third stage of a Pegasus launch vehicle. It was injected into an elliptical orbit of 362 Km by 2544 Km at a 70 degree angle of inclination on August 3, 1994. The orbital period is about 115 minutes, and the perigee and apogee precess around the world about once a year. The APEX orbit is excellent for CRUX objectives, visiting regions populated with galactic cosmic rays and trapped protons (the Van Allen belts, including the South Atlantic Anomaly). The orbit parameters also define a region which covers the venues of most near earth satellite missions. There are three other experiments on APEX, one them being a companion instrument, CREDO (Cosmic Ray Environment and Dosimetry) experiment. CREDO measures both the total dose acquired in flight and the incidence and LET (Linear Energy Transfer) of encountered particles.

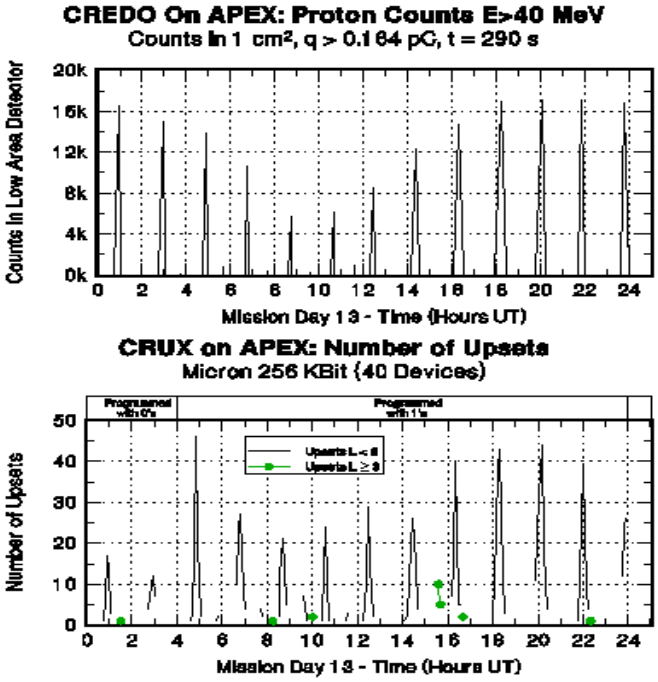
SYSTEM OPERATION

At system power initialization the parts are programmed to a logic state of "1". Then every five minutes thereafter all the memory cells are interrogated to determine if any have been upset. The site of each upset cell is stored in memory, and once a day these data are downloaded to a ground station. On alternate days the memories are reprogrammed to the opposite logic state, and this reprogramming and readout continues for the life of the mission.

RESULTS -- ENVIRONMENT CORRELATION

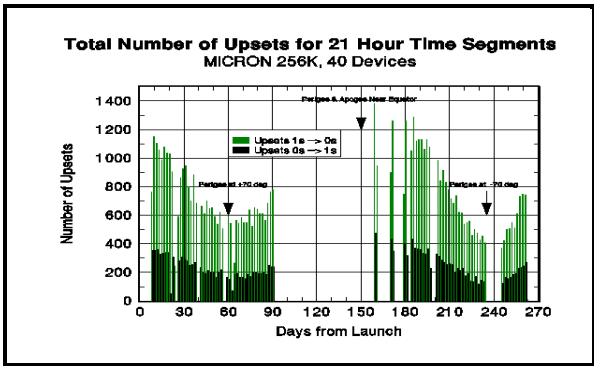
Figure 1 shows a daily plot of the proton fluence encountered by APEX during the first 270 days of the mission as calculated using the actual APEX orbital positions and the published AP-8 model for protons in space. The slow, long-term change in the magnitude of the daily fluences reflects the orbit precession around the world, and the small daily changes reflect changes due to the amount of time spent in regions of high proton fluxes. The gaps in calculated fluences in the middle of the figure means that at these times the spacecraft experiments were powered down while severe buss systems problems on APEX were being addressed. Figure 2 shows the total number of upsets experienced on a daily basis by the Micron 256K SRAM for the same period. Notice the high correlation with Figure 1 shown by a similar slow rise and fall with time. The gaps in data again reflect when CRUX was powered down. Note also the sharp difference on alternate days in the magnitude of upsets. This is due to the fact that every other day the memory cells were programmed either to a logic "1" or a logic"0" state. The daily difference in upsets thus indicates that this device type has a higher propensity to upset when in a "1" state than when in a "0" state. Five other SRAM types flown as DUTs on CRUX also exhibited similar variations in magnitude of daily upsets and all track with the daily proton fluences. Most also demonstrated sensitivity to upsets depending on logic state, but to a greater or lesser degree.

Figures 1 and 2



While Figures 1 and 2 showed the daily fluences and upsets and an apparent high correlation between the two, Figure 3 picks out one day and looks at fluences and upsets on an orbit by orbit basis. Once again a slow variation is seen in both, as the orbit precesses longitudinally and the amount of time spent in high flux regions changes, with upsets varying accordingly. Note also the big jump in upsets in the third orbit at hour 5. Sometime between orbits two and three the parts were reprogrammed from a logic "0" state to a logic "1" state, and the number of upsets jumped accordingly. Similar correlations were seen looking at other days for this part type and at days for the other part types.

Figure 3



While Figures 1, 2, and 3 show excellent correlation between proton fluences and upsets on a temporal basis,

Figures 4 and 5 show equally good correlation on a spatial basis. Here the upsets which occurred were sorted into altitude bins and plotted on a world map grid. Figure 4 is the 1250 to 1350 Km altitude bin and the density of upsets is greatest in the region of the South Atlantic Anomaly (SAA) where proton fluxes are highest. This is shown by the overlays of high flux contour lines on the same map. Figure 5 is for the 1750 to 1850 Km bin, and once again the upset density is highest where the proton flux contour lines are highest. Notice that the SAA has lost its sharp definition at this altitude and now blends in with the rest of the Van Allen belt. Though not shown, at lower altitudes the SAA is more sharply defined, and this is reflected by the highest density of upsets.

Figure 4

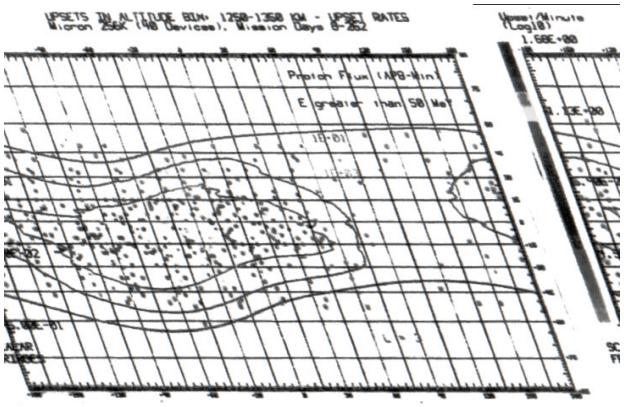
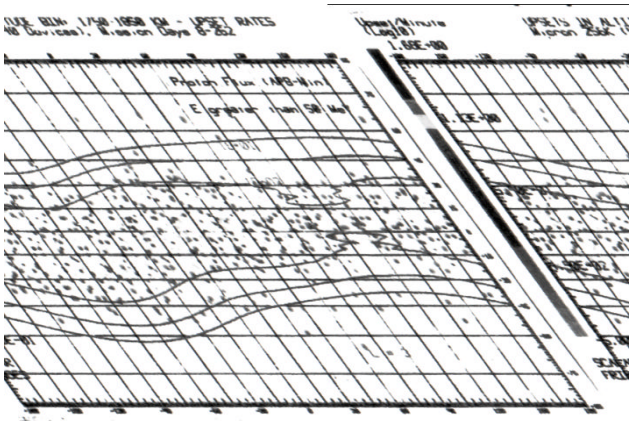


Figure 5

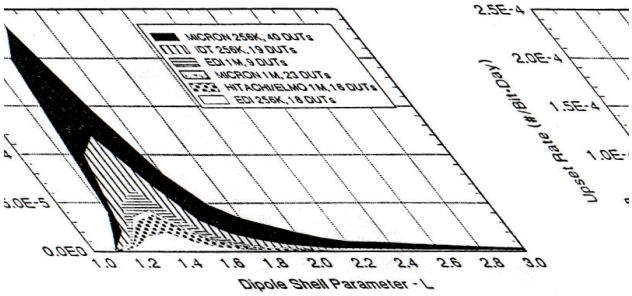


The foregoing correlations are strong evidence that upsets in the newer part types are dominated by protons. This is contrary to thinking just a few years ago, when the concern was that heavy ion galactic , cosmic rays were the primary cause of upsets, and thus the upset problem is more serious than previously thought. Closer examination of figure 3 shows a few upsets did occur between the peaks of high proton fluences. It was determined that these all occurred at high L-shell values, i.e., outside high flux domains. These upsets are thus concluded to have been caused by heavy ions. It is interesting to note that while while 40% of orbital time was spent in the domain of heavy ions, only 3% of the upsets occurred there, while 97% of upsets occurred during the 60% of the time spent in proton flux domains.

RESULTS -- PARTS RESPONSES

The six static random access memory (SRAM) types of microcircuits used as DUTs on CRUX are listed in Table 1. The daily upset rates by part type are shown in Figure 6. As might be expected, upset sensitivities vary, with more than an order of magnitude difference between the hardest and softest types here. However, all types had the highest upset rates at the same L-shell value of about 1.4.

Figure 6



A disturbing result of the data analysis was the large device to device variation within each of two of the six part types. This is shown in table 2. For each part type, the manufacturers had promised to supply devices made from the same mask set. This was to assure lot homogeneity and the applicability of the error rate prediction models to the data. The mask set details all the physical dimensions, and these in turn have a first order effect on upset sensitivity. Table 2 shows relatively tight distributions for all the types except the Micron 1M and the EDI 256K. These two types show high ratios of number of upsets of the most sensitive device to the least sensitive device within each part type, high values of standard deviations, and a high percentage of the standard deviation to the average number of upsets, all of which argue that the lot is not homogeneous, not all made from the same mask set.

Table 1: SRAM Test Devices on CRUX

Part Type	Manufacturer	Technology	Chip Size	# of Devices	Total Bits
MT5C1008CW25	MICRON	NMOS/CMOS	128K x 8	23	24,117,248
88130L45PC	EDI	NMOS/CMOS	128K x 8	9	9,437,184
ZQ0405 4628128	HITACHI/ELMO	NMOS/CMOS	128K x 8	16	16,777,216
MT5C2568CW-25	MICRON	CMOS	32K x 8	40	10,485,760
8832C120C1	EDI	CMOS	32K x 8	18	4,718,592
71256L100DB	IDT	NMOS/CMOS	32K x 8	19	4,980,736

Table 2: Upsets for CRUX Part Types

Part Type	Number of Upsets			Std Dev	Ratio Max:Min	% STD DEV Ave # Upsets
	Min	Ave	Max			
MICRON 1M	346	1687	3625	873	10:1	52
EDI 1M	2046	2307	2503	172	5:4	7.5
HITACHI/ELMO 1M	1261	1370	1568	97	5:4	7
MICRON 256K	1732	2376	3128	254	9:5	11
EDI 256K	44	171	523	160	12:1	94
IDT 256K	930	1113	1329	116	3:2	10

The differing sensitivity to being upset, depending on programmed logic state, was noted earlier. Table 3 shows how this characteristic varies with device type. Note that the Micron 1M is almost 50 times more sensitive to upset when programmed to a "1" state than when programmed to a "0" state! The Micron 256K and the IDT 256K show about a 3X greater sensitivity in a "1" state, and the Hitachi 1M about a 2X increase. At first glance the EDI 1M and the EdI 256K show little difference in state dependency, but note the standard deviation for the latter part type. Further analysis showed a very wide variation from device to device in this part type. Two of the 18 devices upset only when programmed to a "1" state, and never upset while in a "0" state. Another eight devices were also more sensitive when in a "1" state, but to a much lesser degree, and the other eight devices were more sensitive (by a ratio of 3:1) when in a "0" state. Both the device to device variation within a part type and the "preferred" logic state to upset are factors which designers might consider in system designs.

Table 3: Sensitivity of CRUX SRAMs to Programmed State

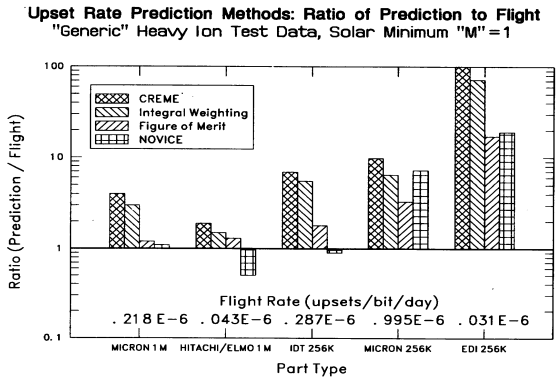
Part Type	% Upsets "1 to 0"	% Upsets "0 to 1"	Std Dev %	Radio "1 to 0" : "0 to 1"
MICRON 1M	98	2	1	49:1
EDI 1M	54	46	1	1:1
HITACHI/ELMO 1M	65	35	5	2:1
MICRON 256K	77	23	3	3:1
EDI 256K	46	54	25	Infinity to 1:3
IDT 256K	77	23	7	3:1

ERROR RATE PREDICTIONS

The earlier stated purpose of CRUX was to try to validate the error rate prediction models. Although early budgets planned for monies to perform ground testing on samples from the flight lots of parts, to date these monies have not been made available. Thus, soon after data reduction started, it was decided instead to use "generic" data, i.e., data which is published in technical journals and exist in parts data banks. Although there would seldom , if ever be, any traceability of the data to determine the manufacturing mask set identification, it was decided to use the generic data to see what the results were. It is important to note that the use of generic data, rather than flight lot part testing, is the standard procedure which many users do routinely employ in making their error rate predictions. It was hoped that we could thus assess the risk of this route by doing likewise. Figure 7 compares predicted upset rates for heavy ions versus measured flight rates on CRUX/APEX. Comparisons are given using four different error rate prediction models applied to five of the six part types. No generic data could be found for the EDI 1M part. Two of the part types have acceptable agreement, i.e., within 4X. Two part types are marginal -- up to 10X off. And one type

has predictions which are totally unacceptable at up to 100X off. Error rate predictions for protons using three different models showed similar results.

Figure 7



CONCLUSIONS

The strong statistical evidence from CRUX/APEX shows that upsets on newer devices are dominated by protons, not heavy ions. If flight lots are not homogeneous, upset sensitivity from device to device within a lot can vary widely and could affect circumvention decisions. Upset sensitivity depending on logic state may be a consideration in circuit designs. In making error rate predictions for critical systems, the use of generic data is discouraged. Although predictions may be good in some cases, users cannot count on this consistently, and the degree of inaccuracy is unknown. For critical applications, users should ground test parts from flight lots, test them as completely as possible, and test as many samples as possible to assure lot homogeneity.

REFERENCES

CRUX/APEX results were presented in 1995 at the Nuclear and Space Radiation Effects Conference (NSREC) in Madison, Wisconsin and at the RADiation and their Effects on Components and Systems (RADECS) Symposium in Arcachon, France. For those interested in a more complete and rigorous discussion of the results, please refer to the NSREC paper published in the IEEE Transactions on Nuclear Science, Volume 42, Number 6, December 1995, pages 1964 through 1974. This paper focuses on the science aspects of the work. The RADECS paper focuses more on the part characteristics effects. It will appear in an issue of the IEEE Transactions on Nuclear Science to be published in the first half of 1996. In addition, there may be more interim reports if required (CRUX/APEX is still operational), and lastly there will be final NASA report published shortly after the end of the mission. Call John Adolphsen or Janet Barth at 301-220-3116 for more information.

JET PROPULSION LABORATORY
PARTS ANALYSES

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Failure Analyses

Log#	MFR	LDC	PART DESC	PART NO.	RESULT
6491	NSC	9149B	Microcircuit, Op-Amp, Quad	ULM124FR	Lid separation
6551	LTN	9028	Microcircuit, Op-Amp, JFET Input	LF156A	Overstress
6551	CDI	8319	Diode, 6.4 V Si Ref.	1N4569A	Overstress
6552	HAR	9016	Microcircuit, Octal, D-Type Flip-Flop	54HCS374	ESD damage
6559	UNT	9447 9508A	Microcircuit, Gate Array, Inter-Subassy Bus	12187-UT25ERISB	Oxide defect

Destructive Physical Analyses

Log#	MFR	LDC	PART DESC	PART NO.	RESULT
6128	HAR	9407	Microcircuit, Rad-Hard, Octal Buffer/Line Driver	54HCS244	Passed
6129	HAR	9407	Microcircuit, Rad-Hard, Dual-D Flip-Flop with Set and Reset	54HCS74	Passed
6377	ADI	9241	Microcircuit, Amplifier High Speed Precision Sample and Hold	AD585S	Failed - Void/Thin Oxide
6482	HAR	9422	Microcircuit, Hex, Schmitt Trigger	54HCS14	Passed
6499	HAR	9503	Microcircuit, Rad-Hard, Inverting 3-to-8 Line Decoder/Demultiplexer	54HCS138	Passed
6501	HAR	9342	Microcircuit, Rad-Hard, Synchronous 4-Bit Up/Down Counter	54HCS193	Passed
6504	HAR	9451B	Microcircuit, Rad-Hard, Octal Buffer/Line Driver	54HCS244	Passed
6506	HAR	9215	Microcircuit, Rad-Hard, Dual-D Flip-Flop with Set and Reset	54HCS74	Passed
6604	LTN	9533	Microcircuit, Ref., Ultra Precision	LTZ1000	Passed

Construction Analyses

Log#	MFR	LDC	PART DESC	PART NO.	RESULT
6547	HAR	9514	Microcircuit, Rad-Tol, 32-Bit Virtual Memory Microprocessor	68T020	OK-Partial
6611	ADI	9430	Microcircuit, A/D	AD42961XD	OK-Partial

Manufacturers:
ADI Analog Devices, Inc.
CDI Compensated Devices, Inc.
HAR Harris Corp.
LTN Linear Technology
NSC National Semiconductor Corp.
UNT United Technologies Microelectronics Center

GODDARD SPACE FLIGHT CENTER PARTS ANALYSES

Listed below are the EEE parts analyses completed by GSFC Parts Analyses Laboratory from 9/11/95 through 3/7/96. The Goddard Space Flight Center reports are available to NASA personnel and current NASA contractors by contacting your NASA project office.

Destructive Physical Analyses

Job Number	Manufacturer	Part Type	Part Number	Date Code	Result
51754	National	Microcircuit	JM38510R75202BCA	9418A	Pass
51755	National	Microcircuit	JM38510R75702BCA	9435A	Pass
51756	National	Microcircuit	JM38510R75101BCA	9427A	Pass
51757	National	Microcircuit	JM38510R75000BCA	9435A	Pass
51777	AVX	Filter	M28861/04-029TB	9442	Fail
51777	AVX	Filter	M28861/04-034TB	9444	Fail
51777	AVX	Filter	M28861/04-035TB	9444	Fail
51782	Deutsch	Relay	TLS26M601	9451	Fail
51782	Deutsch	Relay	TLS26F2105	9448	Fail
51784			JT06RE-24-2PC Cable	8828	*
51786	National	Microcircuit	JM38510/75204BCA	9442A	Pass
51787	PPC	Transistor	JANTXV2N5005P	9451	Pass
51788	PPC	Transistor	JANS2N3749	9427	Pass
51789	Microsemi	Diode	JANS1N6322	9142A	Pass
51793	TI	Microcircuit	JM38510/31402BEA	9522B	Pass
51794	Deutsch	Relay	TLS12F7017	94-48	Fail
51798	Motorola	Transistor	JANTXV2N6277	9447	Fail
61416	Optek	Transistor	JANTXV2N5794U	9245	Pass
62304	Spectrum Control	Filter	M15733/58-0002	9535	Fail
62307	SSDI	Diode	SPD5818	9305	*
62309	Spectrum Control	Filter	M15733/58-0002	9430	Fail
62325		Transducer	154005G		*
62328	AVX	Capacitor	SV09KC332KAA	9411	Fail
62334	Harris	Microcircuit	IH5108MJE/883B	9052	Pass
62336	Dale		CFR-56 1.0 ohm	9442A	*
62336	Dale		CFR-56 8.0 ohm	9529A	*
62338	Microsemi	Diode	JANS1N6324	9435	Pass
62339	Microsemi	Diode	JTXV1N6310	8504	Pass
62340	Microsemi	Diode	JTXV1N6316	8939	Pass
62341	National Semi. Corp.	Microcircuit	5962-9218601M2A	9441A	Pass
62342	NSC	Microcircuit	5962-8755401BEA	9537A	Pass
62343	NSC	Microcircuit	JM38510/76302BEA	9537A	Pass
62344	T.I.	Microcircuit	5962-9093201M2A	9315A	Pass
62345	T.I.	Microcircuit	5962-88685032A	9532A	Pass
62346	Marconi/GEC Plessey	Microcircuit	DMAR7001FBDAB	9534	Fail
62348		Capacitor	CCR05CK2R2CS	9013	Pass
62350	SCN	Diode	JANTX1N6059A	9536	Pass
62351	Interpoint	Filter	5915-9500401HXC	9539	Pass
62352	Interpoint	Microcircuit	5962-9316301HXC	9542	Pass
62356	EG&G		SGD-100A	D2369	Pass
62357	Nat'l Semiconductor	Microcircuit	M38510/75601BRA	9539	Pass
62358	AVX	Capacitor	87106-065	9540	Fail
62359	Microsemi	Diode	JANTXV1N6122A	8515	Pass
62361	NSC	Microcircuit	5962-9218601M2A	9507A	Fail
62362	Ratheon	Microcircuit	M38510/11201BCA	9306	Pass
62363	Loral	Microcircuit	167A690-347	9539	Pass
62365	Deutcsh	Diode	T05	Unknown	Fail

62368	AVX	Capacitor	87106-027	9537	Pass
62369	Q-Tech	Crystal	SMEX-5955-03/11		Fail
62370			154005G		Fail
62373	Semicon	Diode	JANTXV1N4486A	8144	Fail
62377	NSC	Microcircuit	M38510/75302BCA	9543	Pass
62378	Unitrode	Microcircuit	UC1717SP/883B	9538	Pass
62379	Optek	Transistor	JANTX2N6989U	9314	Fail
62385	Xicor	Microcircuit	X28VC256EMB-55	9452	Pass
62387			154005G		Fail
62388	Unitrode	Transistor	2N5552	8403	Fail
62389	NSC	Microcircuit	5962-8973601CA	9535	Pass
62393	NSC	Microcircuit	5962-8968801EA	9531B	Pass
62394	NSC	Microcircuit	M38510R75201BCA	9444A	Fail
62395	Analog Devices	Microcircuit	M38510/13502BPA	9440	Pass
62396	Harris	Transistor	FRL913OR3	9504	Fail
62397	Optek	Transistor	JX2N5796U	9314	Pass
62399	Dale	Resistor	M8340106K2700GG	9544E	Pass
62400	Dale	Resistor	M8340106K24R0GG	9544B	Pass
62404	PTC	Transistor	2N4150	9126	Pass
62406	NSC	Microcircuit	5962-89682013A	9326A	Pass
62407	Semicon	Diode	JANTXV1N5907	9311	Pass
62408	Microsemi	Diode	JANTXV1N6328US	H9530	Pass
62409	Optek		JANTXV4N24AU	9336	Fail
62410	H.P.	Microcircuit	5962-89785022A	9315A	Pass
62411	Ohmtek	Resistor	87016C1002FC	9312	Pass
62412	CDI	Diode	JANTXV1N4622UR-1	9141A	Fail
62413	(CCYL)	Diode	JANTXV1N5614	9114	Pass
62415	NSC	Microcircuit	5962-9218301M2A	9543A	Pass
62420	Solis State, Inc.	Transistor	2N5552	9604	Fail
62426	Ohmtek	Resistor	87016A1001FC	9420	Pass
62427	UTMC	Microcircuit	5962-8957701ZA	9552	Fail
62435	NSC	Microcircuit	M38510R75703SRA	9450	Pass
62438	Analog Devices PMI	Microcircuit	5962-8967001CA	9519A	Pass
62441	Optek	Transistor	JANTX2N6989U	9525	Pass
62443	Linfinity	Diode	JANTXV2N6510	9350	Pass

Items marked "" in the result implies that the DPA has become an evaluation*

Failure Analyses

Job Number	Manufacturer	Part Type	Part Number	Date Code
51752	SEI	Microcircuit	7820RPDE	9234
51761			CCD Assembly	
51792	AVX	Filter	M28861/04	
62319	Allegro	Microcircuit	UDS2981H-883	9246
62320	Harris & H.P.		PCA#1	
62322	Micro Ohm		RJ715	
62326	JPL supplied	Capacitor	Cap Chip 5100 PF	8744
62330	Linear Tech. Corp.	Microcircuit	JM38510/12407SGA	9122
62332			AM7969-125DC	
62333	Dale	Resistor	RWR81S2R05FS	
62337	Kemet	Capacitor	Chip Ceramic Caps	
62367		Transistor	2N5087	9033
62371	Littlefuse	Fuse	FM08	
62372	Semicon	Diode	JANTXV1N4486R	8144
62374	Motorola	Transistor	JANTXV2N2219A	8410 8218
62381	CE	Microcircuit	570087-1	
62391	NSC	Microcircuit	95103-004	

62403	Genicom	Relay	M39016/31-003M	
62360			HCS14DMSR	
62366		Diode	JANTX1N4967	8208

Evaluations

Job Number	**Manufacturer**	**Part Type**	**Part Number**	**Date Code**
51797	STC	Transistor	JANTXV2N6277	9528
62313	Micropac		61055-301	9508
62349		Capacitor	Capacitor	
62355			Taxi Chip	
62383	SSDI		SC7D04-001FSA	9424
51773	National	Switch	CS-3756C-26	

GIDEP & NASA ADVISORY IMPACT REPORT

NASA Advisories, GIDEP Alerts, Problem Advisories, Safe Alerts, Product Change Notices,
Diminishing Source Notices and Agency Action Notices related to EEE parts
October 1995 - February 1996

Document #	Date	Part No.	Mfr.	Summary / Part Type
AAN-U-95-100	9/25/95	N/A	N/A	DESC has established a new Commercial And Government Entity (CAGE) code, 037Z3, for use with all DESC drawings.
AH6-C-96-01	10/13/95	MULTIPLE	National	The manufacturer is changing the top mark of all NEW compliant QML products.
AH6-D-96-01	10/13/95	MULTIPLE	National	Manufacturer is discontinuing subject microcircuits.
AH6-D-96-02	10/18/95	DH0034D-MIL	National	Manufacturer is discontinuing subject microcircuit.
AX8-A-96-01	10/19/95	MIL-C-38999 SERIES I, II, & III	Matrix Science Connectors	Connectors might not fully satisfy the requirements for contact retention, as specified in paragraphs 3.23 and 4.7.19 of MIL-C-38999. The primary concern relative to contact retention or location is the possibility of electrical discontinuity.
BP6-C-96-01	10/13/95	N/A	Harris	Harris changed their "top side" brand traceability code.
BP6-C-96-02	10/19/95	ICL7642CMJD	Harris	Harris is issuing this document to advise you of the package change being made.
BP6-C-96-03	10/19/95	MULTIPLE	Harris	Harris is changing their wafer process.
BP6-C-96-04	10/19/95	HSX-6664RHXX	Harris	Harris is making a data sheet change.
EA-A-95-01A	10/2/95	MANY JAN, JANTX, AND JANTXV DIODES	BKC	This amendment confirms that some product with date codes 9103thru 9513 may not sustain the full rated surge current. BKC recalled distributor stock & stopped shipments as of 3/30/95.
EA-D-95-57	9/22/95	MULTIPLE	Harris	Manufacturer is discontinuing subject microcircuits.
EA-D-95-60	9/25/95	MULTIPLE	National	Manufacturer is discontinuing subject microcircuits.
EA-D-96-01	10/5/95	BF871	Philips	Manufacturer is discontinuing subject transistor.
EB7-P-96-01	10/11/95	MULTIPLE	Ultronix	Due to excessive failures in Group "C", Subgroup 1 testing (Load Life) per MIL-R-39005, Ultronix is required to reduce our failure level on the products, outlined

Document #	Date	Part No.	Mfr.	Summary / Part Type
				below, in the higher value range from an "R" (.01%/1000 hr.) to a "P" (.1%/1000 hr.) level effective lot date code (LDC) 9345 to current.
LX-P-95-01	9/26/95	M39006/21-0142, M39006/09-8717, M39006/09-8740	North American Capacitor	The use of clear insulating sleeving on capacitors allows cleaning solvents and flux to become entrapped under the sleeving. After the capacitors are installed they are then cleaned. The effect of this cleaning process results in degradation of the marking and oxidation of the metal cases.
U8-P-95-02	10/16/95	JANTX2N6770	IRC	Device (T-4 case outline), exhibits inconsistent case/lead sealing glass fill (volume), which results in (random) glass protrusion beyond the specified header seating plane. When this condition occurs, the use of this part in conjunction with a ceramic insulator pad results in damage to both the pad and the package case/lead sealing glass.
VV-D-95-19	9/26/95	MULTIPLE	Phillips	Manufacturer is discontinuing subject microcircuits.
VV-D-95-20	9/27/95	MULTIPLE	Philips	Manufacturer is discontinuing subject microcircuits.
X2-D-95-25	9/22/95	MULTIPLE	Harris	Manufacturer is discontinuing subject microcircuits.
X2-D-96-01	10/16/95	MULTIPLE	TI	Manufacturer is discontinuing subject microcircuits.
X2-D-96-02	10/17/95	MULTIPLE	Philips	Manufacturer is discontinuing subject microcircuits.
AH6-C-96-02	11/08/95	Multiple	National	The manufacturer is reporting a process change (die shrink). The conversion of the die to a "true-dual amplifier" layout has resulted in a 45% die size reduction.
AH6-C-96-03	11/17/95	Multiple	National	The test limits for the output sink current test are being changed to correct a severe yield loss at the -55/+125 degree C final test operation.
AH6-P-96-01	11/09/95	DS26LS32ME/883 DS26LS32MJ/883 DS26LS32MW/883	National	The manufacturer is advising participants of an error which affects the AC parameter test condition for the capacitance load of listed part numbers.
BP6-C-95-05	11/15/95	MULTIPLE	Harris	The manufacturer is changing the bonding wire diameter for certain analog products.
C1-A-95-01	11/13/95	87106-241, 87106-265 87106-265, 87106-325	Johanson Dielectrics Inc.	The ceramic switch mode power supply capacitors were received from the manufacturer with "j" lead bend dimensions exceeding the maximum value of 0.080 inches (0.070+/-0.010).

Document #	Date	Part No.	Mfr.	Summary / Part Type
CE9-C-96-01	10/31/95	SMJ320C30, SMJ320C31, SMJ320C40, MC1558, SNJ54LVT245	TI	The manufacturer has made recent changes to tips military integrated circuits. Changes to electrical datasheets, non-electrical and/or mechanical changes.
CE9-D-96-01	11/21/95	MULTIPLE	TI	Manufacturer is discontinuing subject microcircuits.
CE9-D-96-02	11/20/95	SNJ54AS21	TI	The device does not maintain a high level voltage at the output with the specified Vih of 2.0V at low temperatures. The manufacturer will cease production rather than correct the problem.
EA-D-96-02	11/02/95	CY7C910-51LMB	Cypress	Defense Electronics Supply Center (DESC) is reporting the discontinuance of this device and their associated national stock number.
EA-D-96-03	11/03/95	MULTIPLE	see description	DESC is reporting the discontinuance of the devices and their associated national stock number: Avantec, Ratheon, U.S.Army, Loral, E-systems Naval Sea Systems Command, Hughes Aircraft
EA-D-96-04	11/07/95	MULTIPLE	Philips, Fairchild, National, Intecolor	DESC is reporting the discontinuance of the devices and their associated national stock numbers.
98FJ3-D-96-01	11/08/95	BT471KPJ80, BT478KPJ80	Brooktree	Manufacturer is discontinuing subject microcircuits.
Q9-A-96-01	11/15/95	MS3400, MS3401, MS3402, MS3404, MS3406, MS3408	Transtechnology Electronics	Front release style MIL-C-5015 connectors, purchased to MS340X with size 16 contact positions (pins and sockets) do not meet MIL-STD-1651 for contact position. The connector insert does not sufficiently support the contacts to meet the contact true position requirement per the MIL-STD.
VV-D-96-01	11/17/95	MULTIPLE	Altera	Manufacturer is discontinuing subject microcircuits.
EA-D-96-05	11/27/95	multiple	Hughes Aircraft Company	Defense Electronics Supply Center (DESC) is reporting the discontinuance of the subject microcircuits and their associated national stock numbers.
EA-D-96-06	12/6/95	multiple	Pollack Corporation	DESC is reporting the discontinuance of the subject switches and their associated national stock numbers.
EA-D-96-07	12/1/95	LM11CN, 5962-01-342-9799	Motorola Semiconductor Corporation	DESC is reporting the discontinuance of the subject microcircuits and their associated national stock numbers.

Document #	Date	Part No.	Mfr.	Summary / Part Type
EA-D-96-08	12/19/95	multiple	National Semiconductor Corporation	DESC is reporting the discontinuance of the subject transistors and their associated national stock numbers.
GU2-D-96-01	12/14/95	multiple	Intel Corp.	Manufacturer is discontinuing subject microcircuits.
EB7-P-96-03	12/18/9	multiple	Sprague North Adams, Inc.	The manufacturer has experienced a military maintenance test failure, (Group B. Subgroup 2, 85 deg C Life for 10,000 hrs.) which exceeded the allowable number of failures on the MIL-C-39006/03-1438 (280D106X8300P), and the MIL-C-39006/03-1434 (280D126X8250P) high voltage hermetic foil. It has been further determined that these lot failures are limited only to 200v, 250v, & 300v, "M" and "P" failure rate product.
U7-D-96-02	12/15/95	multiple	Hewlett-Packard	Manufacturer is discontinuing subject microcircuits.
U7-S-96-01	12/20/95	KMH200VN681M30X30T2	United Chemi-con	A faulty lot of electrolytic capacitors on the power supply boards used in the Hewlett-Packard (HP) 70001A-H10, 70001A, 70004A instruments may leak electrolyte across high voltage traces leading to a potential fire hazard.
AH6-C-96-04	1/12/96	Multiple	National Semiconductor Corp.	Microcircuit process/ product change notification.
AH6-D-96-03	1/3/96	LM7709H-MIL, LM7709, LH0071-2H-MCP	National Semiconductor Corp.	Manufacturer is discontinuing subject microcircuits.
CE9-C-96-02	1/11/96	Multiple	Texas Instruments Inc.	The manufacturer has eliminated 100% burn-in on the linear microcircuits.
CE9-C-96-03	1/11/96	Multiple	Texas Instruments Inc.	The manufacturer has made changes (electrical and/or mechanical to it's military integrated circuits.
CE9-C-96-06	1/26/96	Multiple	Texas Instruments Inc.	The manufacturer has eliminated 100% burn-in on the LBC devices.

Document #	Date	Part No.	Mfr.	Summary / Part Type
CM2-C-96-01	1/16/96	AD7672, 5962-8965501LA, 5962-8965502LA	Analog Devices Inc.	The manufacturer has issued a product change notice to advise of a die fabrication redesign used for the military microcircuits.
EA-D-96-10	1/16/96	SN75189N3, 5962-01-248-2324	Texas Instruments Inc.	Defense Electronic Supply Center (DESC) is reporting the discontinuance of the subject microcircuits and their associated national stock numbers.
E8-A-96-01	1/22/96	403148 , FSC-5935, M83513/3-05, M83513/3-06 MIL-C-83513	Cristek Interconnects Inc.	Internal crimp defects caused increased contact resistance and/or open electrical circuits with time/temperature exposure.
K8-A-96-01	1/9/96	FHN28WB, FHN-41WB 5920-00-964-4384, 5920-00-172-3149 , MIL-F-19207/17-002 , MIL-F-19207/25-002	FIC Corporation	Numerous occurrences of fractured mounting threads on the subjectfuseholders have been experienced.
WF-A-96-01	1/9/96	Multiple	Amphenol Corporation	During connector mating the electroless nickel plating was peeled off of one size 19 receptacle by the mating coupling nut.
VV-D-96-03	1/6/96	Multiple	GEC Plessey Semiconductor Inc.	The manufacturer is discontinuing subject microcircuits.
AH6-C-96-05	2/13/96	JAN, SMD, -QML, /883 QB,-MIL MIL-STD-883	National Semiconductor	Microcircuit package marking change notification. Laser marking will be the new standard process flow.
BN8-D-96-01	2/13/96	Multiple	Philips Semiconductor	The manufacture is discontinuing subject discrete and integrated circuit devices..
BN8-D-96-02	2/13/96	Multiple	Philips Semiconductor	The manufacture is discontinuing subject discrete and integrated circuit devices.
BP6-C-96-06	1/24/96	Multiple	Harris Corp.	The manufacturer is changing its datasheets for the subject devices.
BP6-C-96-07	1/31/96	N/A	Harris Corp.	The manufacturer is changing its SEM inspection criteria as allowed under the MIL-PRF-38535 QML program.

Document #	Date	Part No.	Mfr.	Summary / Part Type
CE9-C-96-04	1/31/96	Multiple	Texas Instruments	Under the provisions of MIL-PRF-38535, the manufacturer is eliminating 100% 25 degree DC/AC testing for the listed ALS and FAST Logic products.
CE9-C-96-05	1/29/96	Multiple	Texas Instruments	Under the provisions of MIL-PRF-38535, the manufacturer has eliminated 100% -55 degree DC/AC testing on the following ABT, AC, ACT, AND BCT logic products.
CE9-D-96-03	1/26/96	Multiple	Texas Instruments	The manufacture is discontinuing subject discrete and integrated circuit devices..
CE9-D-96-03	2/22/96	Multiple	Texas Instruments	The manufacture is discontinuing subject discrete and integrated circuit devices..
CE9-D-96-04	2/22/96	Multiple	Texas Instruments	The manufacturer is discontinuing subject microcircuits.
CE9-P-96-01	2/9/96	Multiple	Texas Instruments	The manufacturer is reporting an error in each of the electrical test programs for the subject microcircuits.
DT6-D-96-01	2/20/96	Multiple	Motorola	The manufacturer is discontinuing subject microcircuits.
EA-D-96-11	2/1/96	05342-40001, 5961-01-147-6918 05342-00008 5961-01-302-3750	Hewlett-Packard	Defense Electronic Supply Center (DESC) is reporting the discontinuance of the subject discrete part numbers and their associated national stock numbers.
EA-D-96-14	2/12/96	Multiple	Hewlett-Packard	DESC is reporting the discontinuance of the subject microcircuits and their associated national stock numbers.
EA-D-96-15	2/13/96	Multiple	Hewlett-Packard	DESC is reporting the discontinuance of the subject transformers and their associated national stock numbers.
FJ5-P-96-01	2/14/96	Multiple	Genicom Corp.	The subject relay has shown only a marginal capability for passing the intermediate current test of MIL-R-36016E. This particular test is a group C test and therefore does not affect failure rate.
Q9-A-96-02	2/26/96	5961-00-324-3078, JANTX1N4469 MIL-S-19500/406	Semicon Components	Damage to four motors was found to be the result of four defective (electrically open) diodes. Further visual investigation found forty (40) fractured diodes in the lot (approx. 16%).

Document #	Date	Part No.	Mfr.	Summary / Part Type
T3-A--96-01	2/20/96	5999-00-284-3970,, M39029/35-274, MIL-C-39029/35-274	Winchester Electronics	Missing or damaged outer barrel sleeves can compromise the two ounce minimum withdrawal requirement of the connector.
VV-C-96-01	2/7/96	Multiple	Electronic Designs Inc.	Microcircuit product (die revision) change notification.
VV-D-96-05	2/14/96	Multiple	ATMEL Corp.	The manufacturer is discontinuing subject microcircuits .
VV-D-96-06	2/15/96	ZR33288, ZR33072, ZR36020, ZR36040, ZR36045	Zoran Corp.	The manufacture is discontinuing subject devices.
VV-D-96-07	2/16/96	Multiple	Motorola	The manufacture is discontinuing subject microcircuits
VV-D-96-08	2/23/96	1A0805Z104Z5V1N	Circuit Components Inc.	The manufacture is discontinuing subject microcircuit.
VV-D-96-04	1/29/96	1SL1, 5930-00-548-7991 1SL7, 5930-00-820-3038	Honeywell Inc.	Manufacture is discontinuing subject switches